SEMIKRON
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Technical Explanation
SKYPER®
42 LJ R

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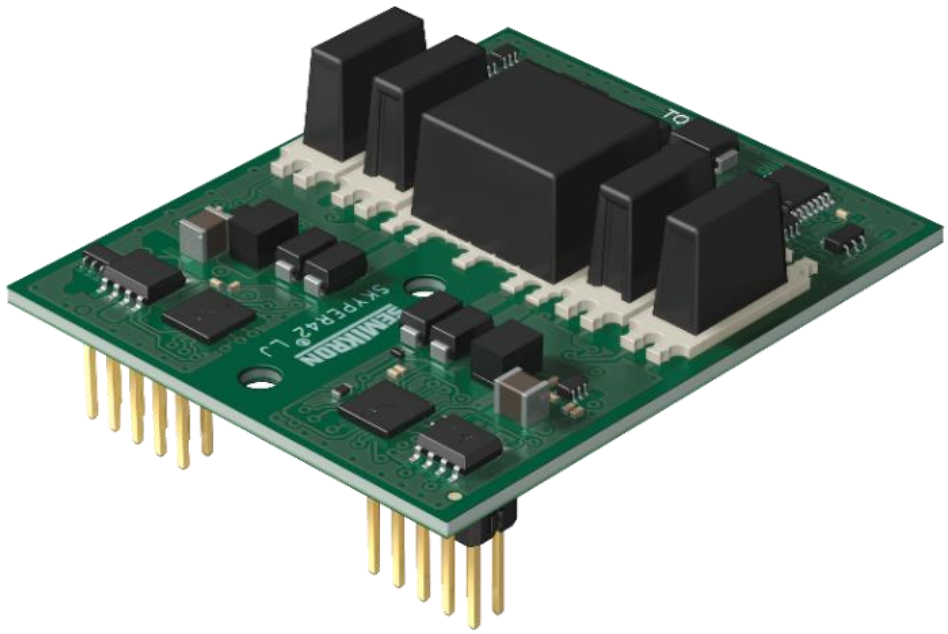
1. Introduction

The SKYPER® 42 LJ R is a two-channel driver core, which combines high output power with highly-integrated ASIC technology in a very compact design. Its high reliability and EMC robustness makes the SKYPER® 42 LJ R suitable for a wide range of applications and sectors of many industries. The SKYPER® 42 LJ R is designed to control semiconductor power modules with gate charges of typically up to 20µC and provides reinforced isolation for operating voltages of up to 1200V. The interaction of the well-coordinated functionality with the integrated safety functions makes the SKYPER® 42 LJ R to a reliable control for power semiconductor modules in standard, multilevel or parallel operation.

Figure 1: SKYPER® 42 LJ R



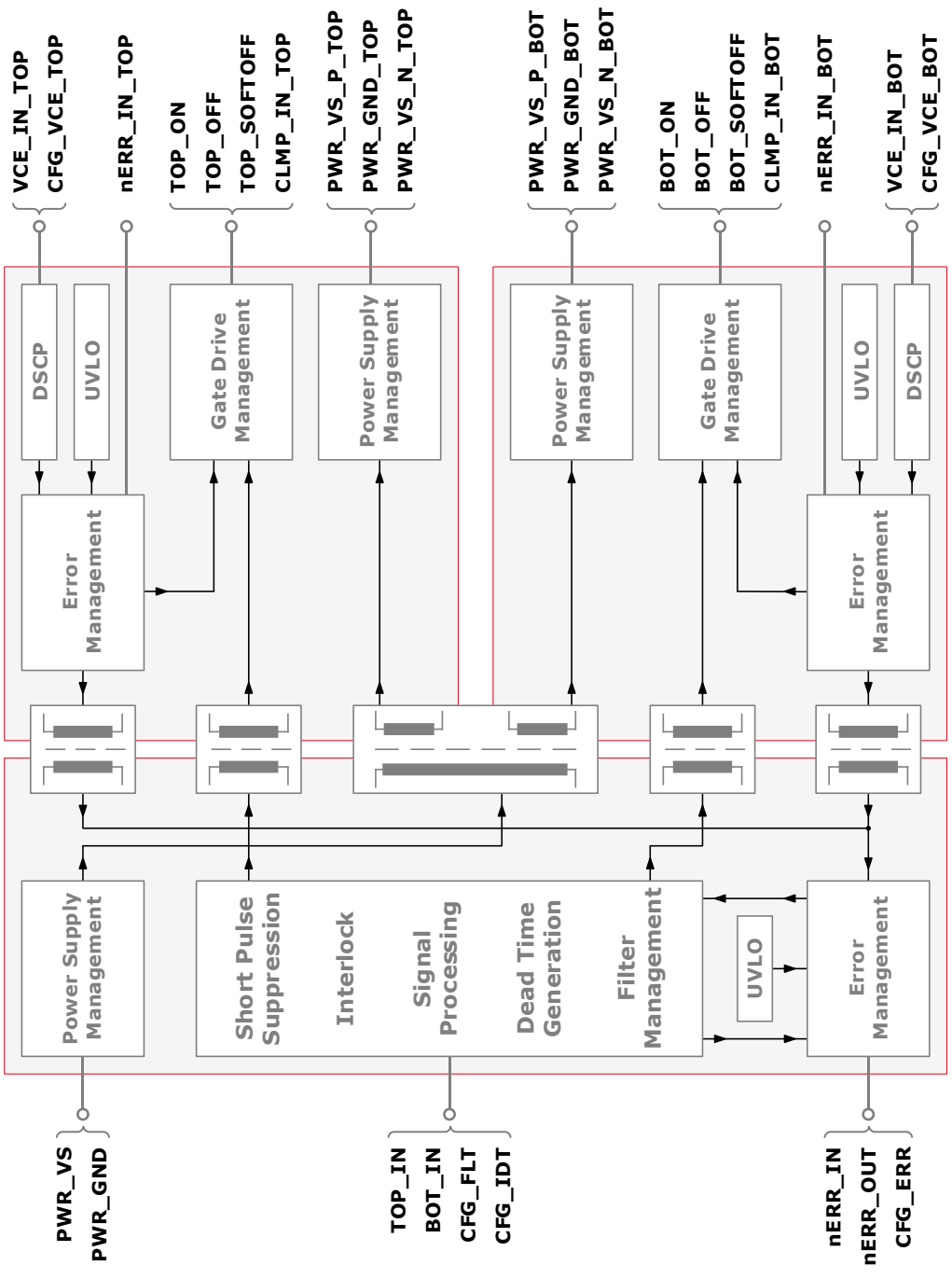
KEY FEATURES

- Two output channels
- 2.75W output power per channel
- ±3 ns jitter per channel
- Fully isolated secondary side power supply
- Separately controlled positive and negative gate voltages
- Selectable filter settings
- Soft turn-off in case of any secondary side error event
- Short pulse suppression (SPS)
- Under voltage lockout (UVLO)
- Dynamic short circuit protection (DSCP)
- MTBF rate > 7.5 Million hours at full load
- Selectable error management modes for standard and multilevel applications

2. Block Diagram and Application Example

2.1 Block diagram

Figure 2: SKYPER® 42 LJ R | Block diagram



2.2 Application example

Figure 3 and Figure 4 show a typical SKYPER® 42 LJ R core setting for operating a semiconductor module in half-bridge configuration. SEMIKRON's highly-integrated ASICs – as utilized on this driver core – enable the SKYPER® 42 LJ R to be easily configured with only a few simple external circuits and in turn reducing the project and development time as well as the cost.

2.2.1 Primary side

Figure 3: SKYPER® 42 LJ R | Application example | Primary side

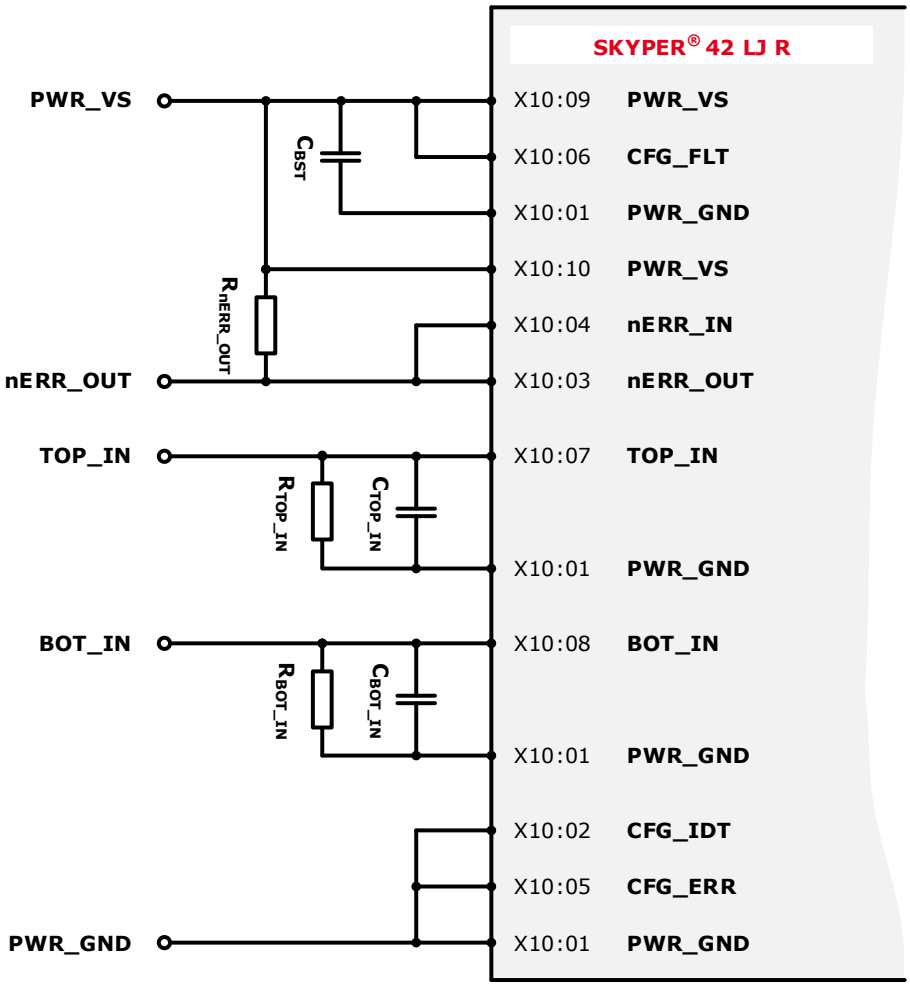


Table 1: SKYPER® 42 LJ R | Application example | Primary side | Recommended values

Component	Value	Remark
C_{TOP_IN} / C_{BOT_IN}	1nF	**Optional** filter capacitors suppressing high-frequency signals. For further information please refer to [3].
C_{BST}	-	**Optional** boost capacitor, dimensioning according to chapter 4.11.
R_{TOP_IN} / R_{BOT_IN}	10kΩ	**Optional** pull-down resistors, for steady off-state of the corresponding output, if no input signal is applied.
R_{nERR_OUT}	4.75kΩ	**Optional** pull-up resistor, **mandatory** if error output is used. Dimensioning according to chapter 4.6

2.2.2 Secondary side

Figure 4: SKYPER® 42 LJ R | Application example | Secondary side

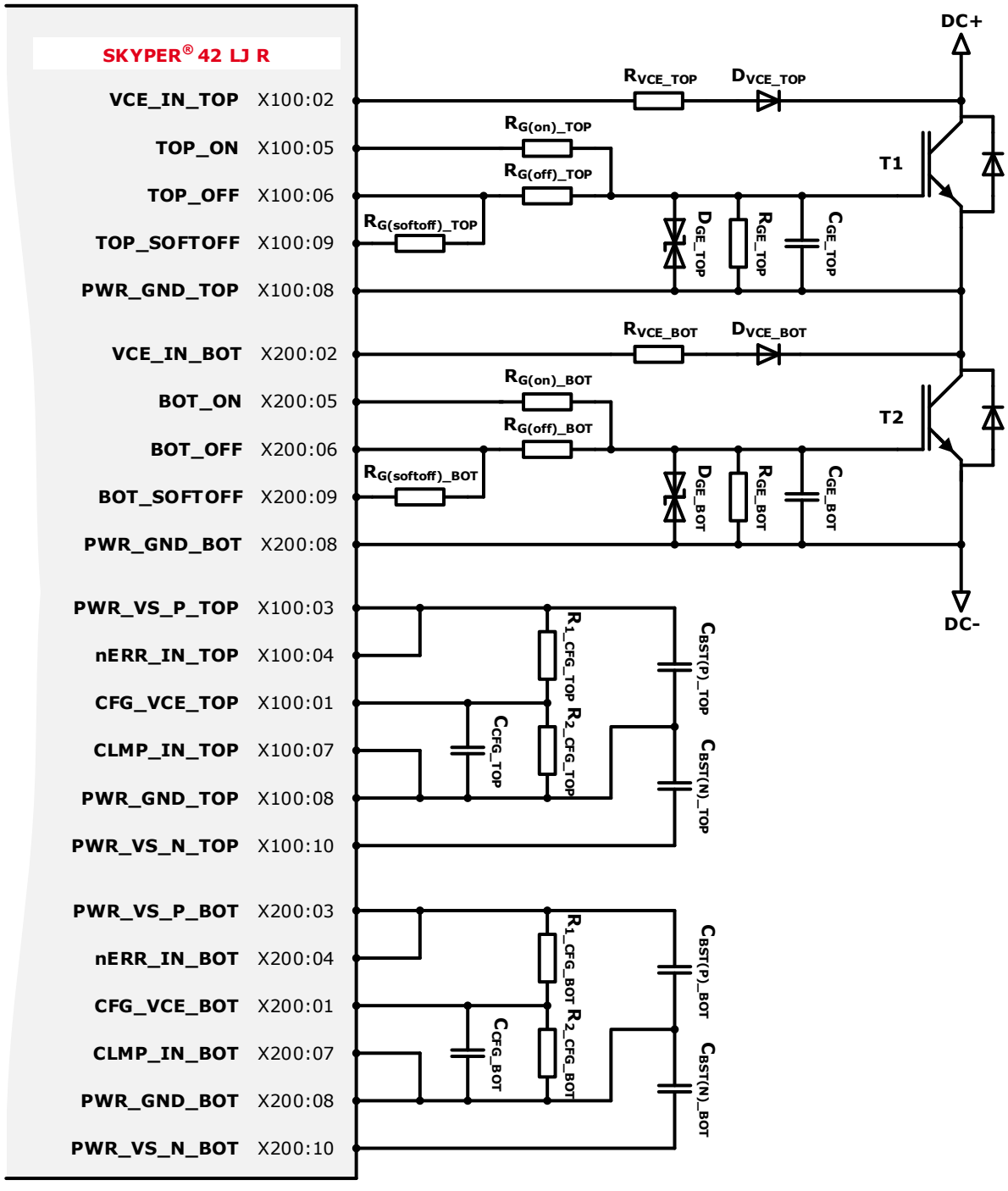


Table 2: SKYPER® 42 LJ R | Application example | Secondary side | Recommended values		
Component	**Value**	**Remark**
$C_{BST(P)\_TOP}$ / $C_{BST(N)\_TOP}$ $C_{BST(P)\_BOT}$ / $C_{BST(N)\_BOT}$	-	**Optional** boost capacitors, dimensioning according to chapter 4.11.
C_{CFG_TOP} / C_{CFG_BOT}	-	**Optional** capacitor to adjust the blanking time $t_{bl(VCE)}$ of the dynamic short circuit protection function. **Necessary**, if DSCP is used. Dimensioning according to chapter 5.5.
C_{GE_TOP} / C_{GE_BOT}	-	**Optional** capacitor to prevent gate oscillation in case of short circuit events or in case of parallel operation of semiconductor power modules. For further information please refer to [3].
D_{GE_TOP} / D_{GE_BOT}	$V_{Rmin} \geq V_{G(on)} + 10\%$	**Optional** suppressor diode to prevent gate voltage overshoots. For further information please refer to [3].
D_{VCE_TOP} / D_{VCE_BOT}	-	**Optional** high voltage diode for V_{CE}-monitoring, **mandatory** if DSCP is used. Dimensioning according to chapter 5.5.
$R_{1\_CFG\_TOP}$ / $R_{1\_CFG\_BOT}$	≥ 10kΩ	**Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5.
$R_{2\_CFG\_TOP}$ / $R_{2\_CFG\_BOT}$	-	**Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5.
R_{GE_TOP} / R_{GE_BOT}	10kΩ	**Optional** resistor to avoid an open gate of the semiconductor, if the driver is not supplied. For further information refer to [3].
$R_{G(off)\_TOP}$ / $R_{G(off)\_BOT}$ $R_{G(on)\_TOP}$ / $R_{G(on)\_BOT}$	≥ 1Ω	**Necessary** resistors to adjust the semiconductors' turn-on and turn-off behavior. Dimensioning according to chapter 4.10.
$R_{G(softoff)\_TOP}$ $R_{G(softoff)\_BOT}$	≥ 1Ω	**Mandatory** resistor to adjust the semiconductors' turn-off behavior in case of soft turn-off. Dimensioning according to chapter 4.10.
R_{VCE_TOP} / R_{VCE_BOT}	511Ω	**Optional** series resistor for V_{CE}-monitoring, **mandatory** if DSCP is used.

Referring to the application example shown in Figure 3 and Figure 4, Table 3 describes the settings made.

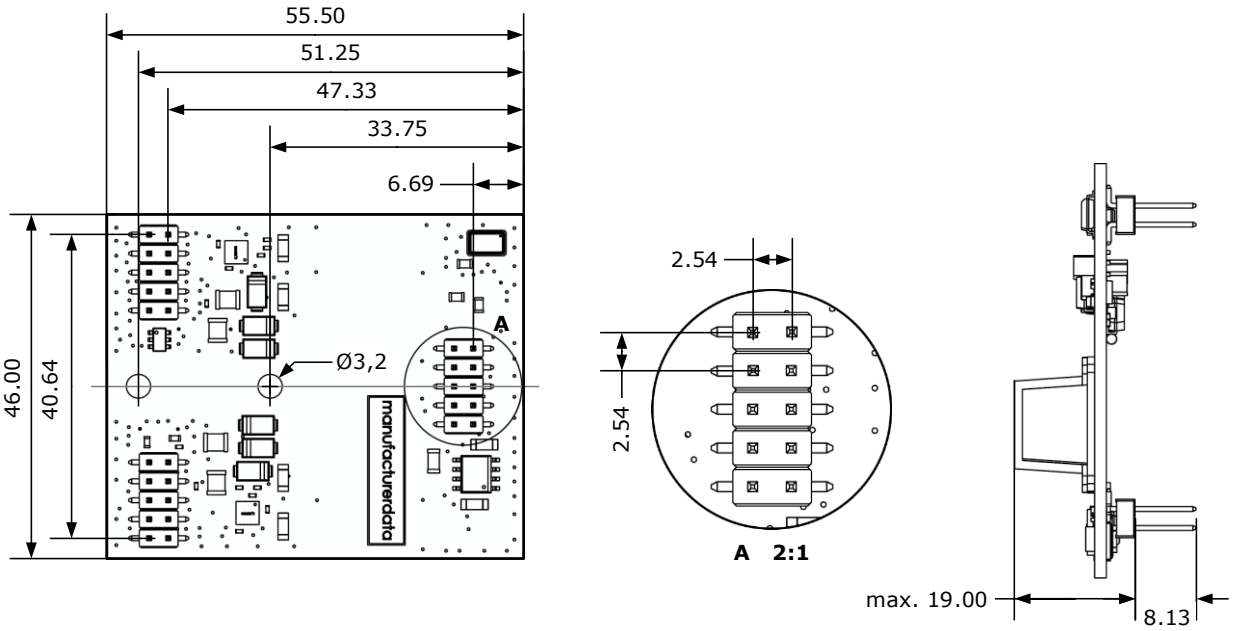
Table 3: SKYPER® 42 LJ R | Application example | Settings

Function	Configuration	Remark	Chapter
Active clamping	Disabled	Disabled by connecting the pins *CLMP_IN_TOP* and *CLMP_IN_BOT* to the corresponding *PWR_GND* pins.	5.6
Bidirectional error (=HALT)	Enabled	Enabled by connecting the pin *nERR_OUT* to pin *nERR_IN*.	4.7
Dynamic short circuit protection (DSCP)	Enabled at both output channels	Enabled by connecting the pins *VCE_IN_TOP* and *VCE_IN_BOT* to the corresponding collectors of the semiconductors through R_{VCE_TOP} , D_{VCE_TOP} and R_{VCE_BOT} ,D_{VCE_BOT}. DSCP configuration via pins *CFG_VCE_TOP* and *CFG_VCE_BOT*.	5.5
Dead time	2µs (typical value)	Selected by connecting pin *CFG_IDT* to pin *PWR_GND*.	5.2
Error mode	Both output channel switch immediately into off-state in case of any error condition.	Selected by connecting pin *CFG_ERR* to pin *PWR_GND*.	5.1
Error propagation delay time	700ns (typical value)	Fixed value.	5.1
External error (HALT)	Disabled at both output channels	Disabled by connecting the pins *nERR_IN_TOP* and *nERR_IN_BOT* to the corresponding *PWR_VS* pins.	5.1
External error propagation delay time	600ns (typical value)	Fixed value.	5.1
Filter	Digital	Selected by connecting pin *CFG_FLT* to pin *PWR_VS*.	5.3
Interlock	Enabled	Enabled by connecting pin *CFG_IDT* to pin *PWR_GND*.	5.2
Jitter	±12.5ns (typical value)	Selected by connecting the pins *CFG_FLT* to pin *PWR_VS*.	4.5
Short pulse suppression (SPS)	390 ns (typical value)	Selected by connecting pin *CFG_FLT* to pin *PWR_VS*.	5.3
Undervoltage lockout (UVLO)	Always active on primary and secondary side	-	5.4

3. Dimensions and mechanical precautions

3.1 Dimensions

Figure 5: SKYPER® 42 LJ R | Dimension drawing



All dimensions in mm. Please consider higher tolerances of connector position according to IPC A 610.
STEP file on request.

3.2 Plug-in connection

The SKYPER® 42 LJ R provides simple electrical and mechanical connection to adapter or control boards by its standard pin headers. The primary side and the two secondary side plug-in connectors are 10 pin dual row 2.54mm pin headers. For a secure mechanical connection of the driver it is essential that the pin headers can be fully supported by the female mating connectors.

SEMIKRON recommends the use of the following female mating connector:

Description	Shape	Manufacturer	Art. no.
(female) RM2.54 10p	SMD 2ROW	Suyin	254100FA

Using SMD type mating connectors allows optimized board layout especially for SEMIKRON's spring contact modules like SEMiX.

3.3 Support post

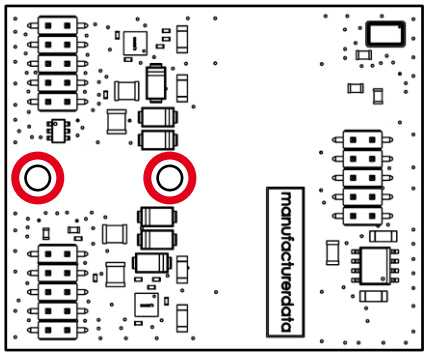
To increase the mechanical connection between the SKYPER® 42 LJ R driver and the adapter board, up to two support posts could be additionally assembled. It is recommended to use at least one support post. If a support post is used, make sure it has the correct length. A support post which is too short bends both the driver and the adapter board when mounted, thus increasing mechanical stress. If the support post is too long, the mating connectors may not fully support the pin header.

The mounting holes of the support post are located in the insulation area between the secondary sides of the driver. To avoid reduction of creepage and clearance distances when utilizing such a support post, the support posts must have a CTI 600 classification at least.

Example of a support post:

Description	Shape	Manufacturer	Art. no.
Nylon support post	Dual lock	Richco	DLMSPM-8-01 (>12mm)

Figure 6: SKYPER® 42 LJ R | Support post



mounting holes for support posts

draft of a supported driver on an adapter board

3.4 Solder connection

The SKYPER® 42 LJ R driver core can be soldered directly onto an adapter or control board. It should be noted that if the driver is placed too close to the adapter or control board, the clearance distances from the driver's primary to secondary side as well as the clearance distances between the secondary sides may be reduced.

Soldering hints

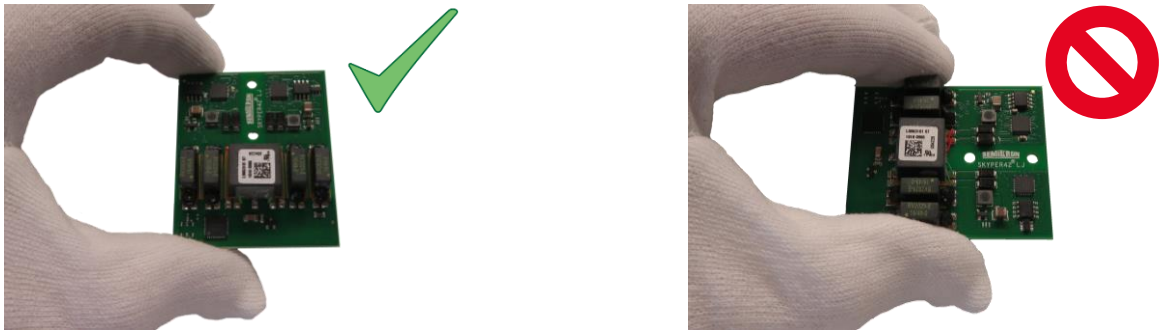
- The solder's temperature must not exceed 260°C and the solder time must not exceed 10 seconds.
- The ambient temperature must not exceed the specified maximum storage temperature of the driver.
- The solder joints should be in accordance to IPC A 610 Revision D (or later) - Class 3 (Acceptability of Electronic Assemblies) to ensure an optimum connection between driver core and printed circuit board.
- The driver is not suited for hot air, reflow or infrared reflow processes.

3.5 Handling instructions

Please ensure electric static discharge protection during handling. The driver should only be removed from its original packaging immediately before mounting. When mounting the driver it has to be ensured that the work is done in an ESD-protected workplace. Persons working with the driver have to wear ESD wristbands, overalls and shoes. If tools are used for mounting, those must comply with ESD standards.

When handling the driver, do not pick up the driver at the transformers. The driver MUST be handled at the PCB sides.

Figure 7: SKYPER® 42 LJ R | Handling instruction

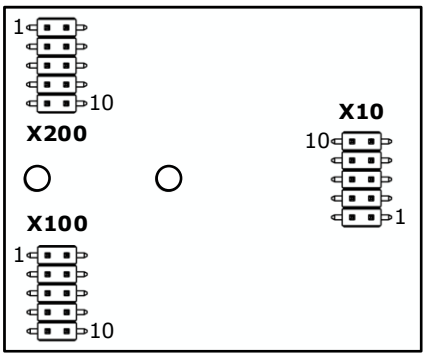


4. Interface Description

4.1 Footprint

The footprint of the SKYPER® 42 LJ R with its primary side pin header X10 and the secondary side pin headers X100 and X200 are shown in Figure 8.

Figure 8: SKYPER® 42 LJ R | Footprint | Bottom view



4.2 Pin assignment

4.2.1 Pin assignment of pin header X10 | Primary side

Table 4: SKYPER® 42 LJ R | Pin assignment – Primary side | X10

Pin	Signal	Function	Specification
X10:01	PWR_GND	Ground potential for power supply and digital signals	To be connected to ground
X10:02	CFG_IDT	Interlock dead time configuration	15V logic; 150kΩ (pull-up) LOW = 2µs interlock dead time HIGH = No interlock dead time
X10:03	nERR_OUT	Error output	Open collector output; max. 18V/15mA (external pull-up resistor needed) LOW = Error HIGH = No error
X10:04	nERR_IN	Error input	15V logic inverted; 150kΩ/10nF (pull-up) LOW = External error HIGH = No external error
X10:05	CFG_ERR	Error behaviour configuration in case of any error condition	15V logic; 150kΩ (pull-down) LOW = Outputs switch off immediately HIGH = Outputs switch off with next turn-off signal at the corresponding input
X10:06	CFG_FLT	Filter configuration for switching signals	15V logic; 150kΩ (pull-down) LOW = Analogue filter ($t_{SPS(ana)}$) HIGH = Digital filter ($t_{SPS(dig)}$)
X10:07	TOP_IN	Switching signal input (TOP)	15V logic; 33kΩ/0.01nF (pull-down) LOW = TOP switch off HIGH = TOP switch on

X10:08	BOT_IN	Switching signal input (BOT)	15V logic; 33kΩ/0.01nF (pull-down) LOW = BOT switch off HIGH = BOT switch on
X10:09	PWR_VS	Driver power supply	Stabilised +15V ±4%
X10:10	PWR_VS	Driver power supply	Stabilised +15V ±4%

4.2.2 Pin assignment of pin header X100 | Secondary side | TOP

Table 5: SKYPER® 42 LJ R | Pin assignment – Secondary side | TOP | X100			
Pin	**Signal**	**Function**	**Specification**
X100:01	CFG_VCE_TOP	V_{CE}-monitoring reference voltage	External voltage divider needed
X100:02	VCE_IN_TOP	V_{CE}-monitoring input	External blocking diode needed
X100:03	PWR_VS_P_TOP	Power supply output, positive voltage	Equal to $V_{G(on)}$ (external buffer capacitors can be connected)
X100:04	nERR_IN_TOP	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X100:05	TOP_ON	On signal path to TOP semiconductor	External gate resistor needed (in consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X100:06	TOP_OFF	Off signal path to TOP semiconductor	External gate resistor needed (in consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)
X100:07	CLMP_IN_TOP	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated TOP_OFF: LOW = TOP_OFF equal to $V_{G(off)}$ HIGH = TOP_OFF floating
X100:08	PWR_GND_TOP	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X100:09	TOP_SOFTOFF	SoftOff signal path to TOP semiconductor	External gate resistor needed
X100:10	PWR_VS_N_TOP	Power supply output, negative voltage	Equal to $V_{G(off)}$ (external buffer capacitors can be connected)

4.2.3 Pin assignment of pin header X200 | Secondary side | BOT

Table 6: SKYPER® 42 LJ R | Pin assignment – Secondary side | BOT | X200			
Pin	**Signal**	**Function**	**Specification**
X200:01	CFG_VCE_BOT	V_{CE}-monitoring reference voltage	External voltage divider needed
X200:02	VCE_IN_BOT	V_{CE}-monitoring input	External blocking diode needed
X200:03	PWR_VS_P_BOT	Power supply output, positive voltage	Equal to $V_{G(on)}$ (external buffer capacitors can be connected)

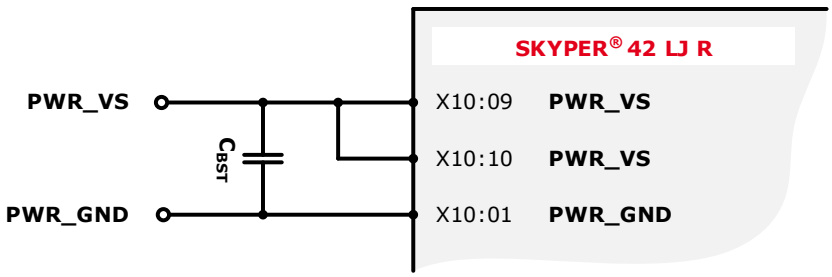
X200:04	nERR_IN_BOT	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X200:05	BOT_ON	On signal path to BOT semiconductor	External gate resistor needed (in consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$)
X200:06	BOT_OFF	Off signal path to BOT semiconductor	External gate resistor needed (in consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$)
X200:07	CLMP_IN_BOT	V_{CE}-clamping input	150kΩ/0.01nF (pull-down) In case of activated BOT_OFF: LOW = BOT_OFF equal to $V_{G(off)}$ HIGH = BOT_OFF floating
X200:08	PWR_GND_BOT	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X200:09	BOT_SOFTOFF	SoftOff signal path to BOT semiconductor	External gate resistor needed
X200:10	PWR_VS_N_BOT	Power supply output, negative voltage	Equal to $V_{G(off)}$ (external buffer capacitors can be connected)

4.3 Power Supply | Primary side

For a proper operation of the SKYPER® 42 LJ R driver core, a power supply of at least 15W/1A shall be connected to the driver's power supply pins. During power-up of the driver turn-on signals shall not be applied to the driver's inputs *TOP_IN/BOT_IN*, otherwise the driver will not leave error state.

Please note, when controlling power semiconductor modules with a gate charge ≥ 2.5 µC external boost capacitors are recommended on the primary side. Dimensioning of the boost capacitors according to chapter 4.11.

Figure 9: SKYPER® 42 LJ R | Primary side | Power supply

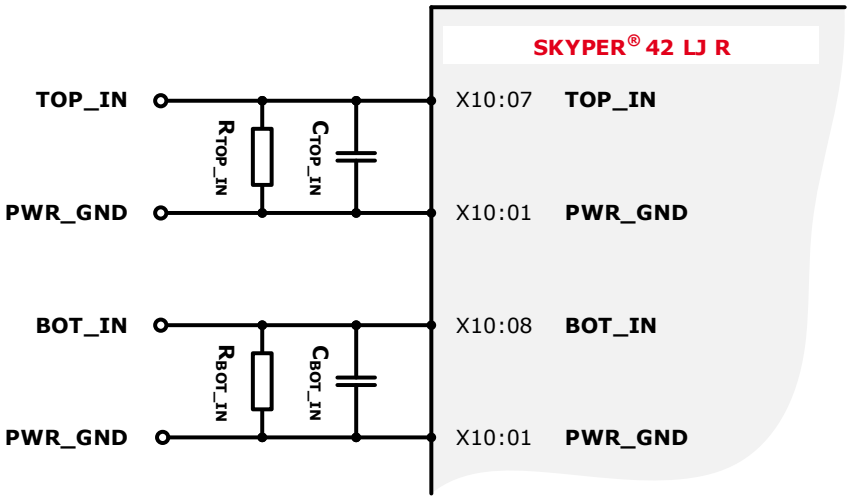


4.4 Gate drive signals | Primary side

The signal inputs *TOP_IN/BOT_IN* of the SKYPER® 42 LJ R driver core have a +15V schmitt trigger logic. A HIGH signal at the input of the driver leads to a switch-on command at the corresponding output of the driver. A LOW signal at the input leads to a switch-off command at the corresponding output. Pulses below 1µs are not allowed.

Short pulses as well as voltage peaks, e.g. caused by interference, are suppressed by the driver and will not be transmitted to the outputs. Further information to the short pulse suppression can be found in chapter 5.3.

Figure 10: SKYPER® 42 LJ R | Primary side | Gate drive signals



When using the driver in environments with high levels of electromagnetic noise, it is recommended to connect a filter capacitor (C_{TOP_IN}/C_{BOT_IN}) of several hundred pico Farads as close as possible to the signal inputs of the driver. Please note that these capacitors affect the propagation delay time of the driver. The R_{TOP_IN}/R_{BOT_IN} resistors pull the inputs to low-level when no control signals are applied. The recommended value of the pull-down resistors is approximately 10kΩ.

Parameter	Min	Typ	Max
Threshold high	-	-	10V
Threshold low	5V	-	-

4.5 Filter selection, jitter and propagation delay time | Primary side

Due to SEMIKRON's highly-integrated mixed signal ASICs the SKYPER® 42 LJ R offers the freedom to select filter type, jitter and propagation delay time to meet specific requirements of the application.

The filter time can be set via the configuration pin *CFG_FLT*. Connecting the *CFG_FLT* pin to the *PWR_VS* pin enables the digital filter employing very low tolerances over the full temperature range.

Especially when using the driver in parallel operation the absolute deviation of the signal propagation delay time from the input to the output is a key parameter. Depending on the settings made the SKYPER® 42 LJ R driver provides a very low jitter of typically ±3ns. Therefore the analogue filter has to be enabled and the driver's internal dead time generator has to be set to inactive. The dead time generator is inactive, if either the interlock feature is disabled via the *CFG_IDT* pin or the dead time of the applied pulse pattern is longer than 2µs. A detailed description of the interlock function and the dead time generation could be found in chapter 5.2.

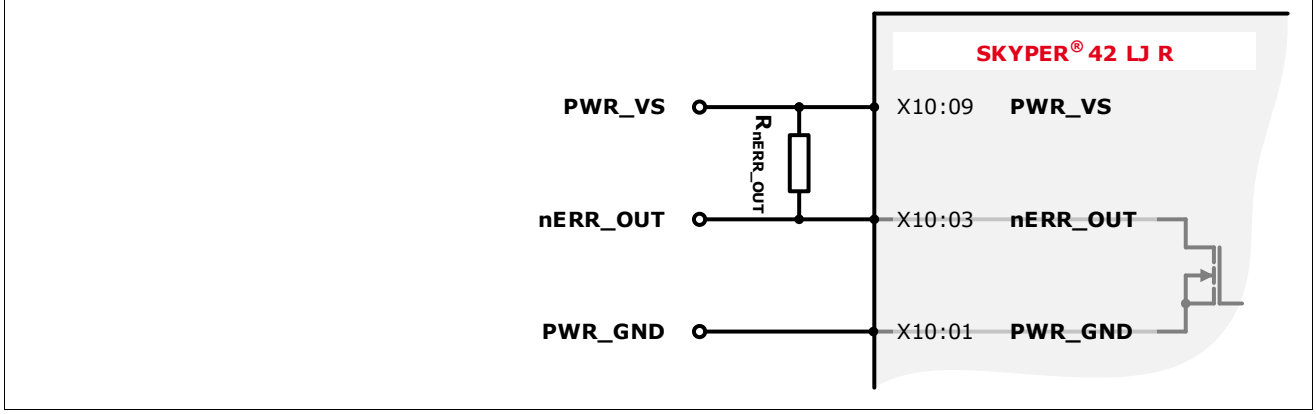
CFG_FLT	*CFG_IDT*	Setting	Filter time	Delay time	Jitter
HIGH	HIGH/LOW	Digital filter	390ns	830ns	±12.5ns
LOW	HIGH	Analogue filter	200ns	500ns	±3ns /±12.5ns
LOW	LOW	Analogue filter	200ns	500ns	±3ns

4.6 Error output | Primary side

The SKYPER® 42 LJ R reports any detected error event at the *nERR_OUT* pin by pulling it to low-level. The error output is an open collector output and requires an external pull-up resistor (R_{nERR_OUT}). The recommended value of the pull-up resistor is in the range of $PWR\_VS/I_{max,nERR\_OUT} \leq R_{nERR\_OUT} \leq 10k\Omega$.
As long as the driver has not been reset the error output will be at low-level.

A detailed description, how to reset the driver to end the error state and resume to operation is described in chapter 5.1.

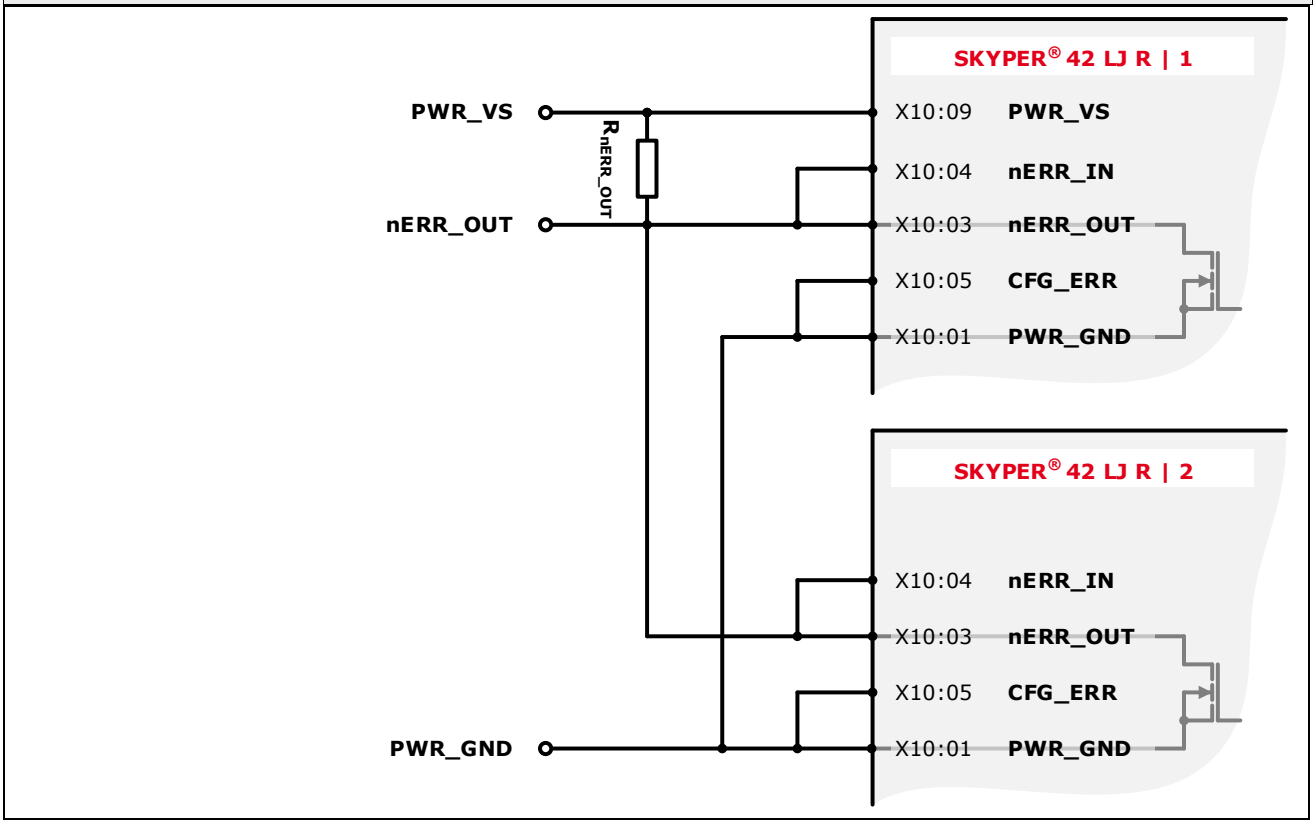
Figure 11: SKYPER® 42 LJ R | Primary side | Error output



4.7 Error input | Primary side

The *nERR_IN* input could be used to report an external error event to the SKYPER® 42 LJ R. If the *nERR_IN* input is pulled to low-level the driver enters the error state. Depending on the error mode configuration, described in chapter 4.8, the driver sets its outputs either immediately or with the next turn-off command to low-level and locks them. After reset, as described in chapter 5.1, the driver is ready for operation, again. If no reporting to the external error input is required, the *nERR_IN* input can be connected to the *PWR_VS* pin or to the *nERR_OUT* pin.
In multiphase or parallel operation the *nERR_IN* input offers the possibility to force the outputs of each driver in the system to off-state and locks them, simultaneously, without the need of an external control unit. Therefore all *nERR_OUT* outputs and all *nERR_IN* inputs have to be connected together forming a common bi-directional HALT line. Additionally, all *CFG_ERR* configuration pins have to be connected to ground potential, as shown in Figure 12. In this configuration, any driver connected to the HALT line can force the outputs of all connected drivers to off-state and locks them, when the driver pulls its *nERR_OUT* output to low-level.
If a specific turn-off sequence is required – as it is common practice in NPC multilevel applications – the configuration pins *CFG_ERR* have to be connected to the *PWR_VS* pins. A low-level of the HALT line locks the outputs of the connected drivers, but does not immediately force them to low-level. The switched-on outputs can be forced to off-state by the controller sending a switch-off command to the corresponding signal inputs *TOP_IN/BOT_IN*.
If the driver is used in environments with high levels of interference, it is recommended to connect a filter capacitor of approx. 10nF as close as possible to the *nERR_IN* pin and the *PWR_GND* pin.

Figure 12: SKYPER® 42 LJ R | Primary side | Error input



Parameter	Min	Typ	Max
Threshold high	-	-	11 V
Threshold low	7.5 V	-	-

4.8 Error mode selection | Primary side

The behaviour of the SKYPER® 42 LJ R driver core on an error event can be selected via the configuration pin *CFG_ERR*.

Connecting the *CFG_ERR* pin to the *PWR_GND* pin forces the driver to set its outputs to off-state immediately when an error is detected. As long as the driver has not been reset the error event is reported at the corresponding terminal and the driver's outputs are kept locked. Whereby, depending on whether an error is detected on the primary or on the secondary side the driver switches off the connected semiconductors via the standard turn-off or the soft-off path. If an error occurs on the primary side the driver will activate the standard turn-off paths of both channels. If an error occurs on the secondary side, the driver will activate the soft-off path of the affected secondary side. The semiconductor connected to the other secondary side will be switched off with the standard turn-off procedure.

If the *CFG_ERR* pin is connected to the *PWR_VS* pin, the driver locks its outputs in case of any error event and, hence, reports the error event at the terminal *nERR_OUT*, but the driver will not be set the outputs to off-state, immediately. The outputs will be set to off-state, when the driver has received a turn-off command at the corresponding signal input *TOP_OFF/BOT_OFF*. Depending on whether an error is detected on the primary or secondary side the driver activates the standard turn-off or the soft-off path, as described above.

Further information related to the primary and secondary error events, as well as on the error reset conditions can be found in chapter 5.1.

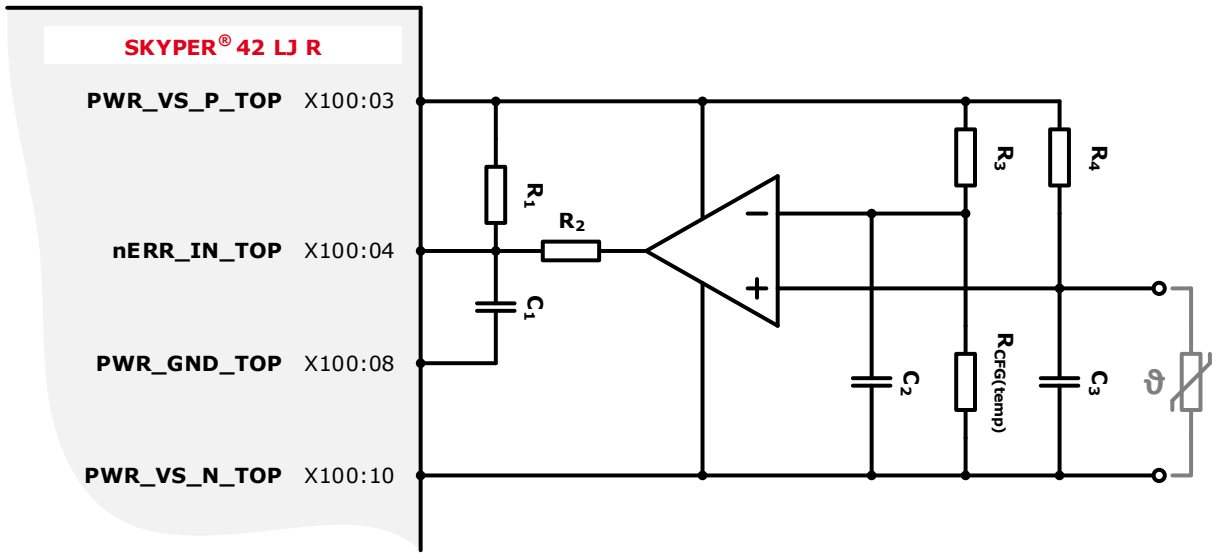
Parameter	Min	Typ	Max
Threshold high	-	-	11 V
Threshold low	7.5 V	-	-

4.9 External error input | Secondary side

Each secondary side of the driver provides an error input (*nERR_IN_TOP/nERR_IN_BOT*) to handle an external error event. These inputs are low active. Pulling one input to low-level forces the driver into error state. The behaviour of the driver in case of an external error event depends on the configuration done via the configuration pin *CFG_ERR*, as described in chapter 4.8.
The external error input is typically used to monitor temperature, current or voltage of modules, phase legs or systems. The error input of the secondary TOP side can be disabled by connecting it to the *PWR_VS_P_TOP* pin the error input of the secondary BOT side by connecting it to the *PWR_VS_P_BOT* pin.

Figure 13 shows a recommended circuitry of an over temperature detection by NTC resistor monitoring. If the voltage at the positive input of the comparator falls below the voltage level at the comparator's negative input the comparator will set the *nERR_IN* input to low-level and will generate an external error event. Assuming that resistor R_3 and R_4 have the same value the comparator's trip level is reached when the value of the NTC falls below the value of $R_{CGF(temp)}$. Please note that the negative supply pin of the comparator is connected to *PWR_VS_N* which has to be taken into account, in case the NTC thermistor is monitored by an external application circuit as well.

Figure 13: SKYPER® 42 LJ R | Secondary side | Example of an external error input circuitry



Recommended values		
Component	**Value**	**Remark**
C_1	1nF	
C_2	100nF	
C_3	1µF	
R_1	30.1kΩ	
R_2	15kΩ	
R_3	30.1kΩ	
R_4	30.1kΩ	
$R_{CFG(temp)}$	-	The value of the $R_{CFG(temp)}$ has to be determined considering the resistance characteristic of the connected thermistor and the desired trip level.

Parameter	**Min**	**Typ**	**Max**
Threshold high	-	-	13 V
Threshold low	2 V	-	-

4.10 Gate resistors | Secondary side

The SKYPER® 42 LJ R driver has three outputs channels at each secondary side (*TOP_ON/TOP_OFF/TOP_SOFTOFF* and *BOT_ON/BOT_OFF/BOT_SOFTOFF*) to provide the possibility of separate optimization of the semiconductor's turn-on and turn-off behavior. By default, the driver uses the *TOP_OFF* and *BOT_OFF* output to turn-off of the semiconductor. The SOFTOFF output will be activated by the driver in case a secondary side error event was detected to ensure a soft turn-off of the connected semiconductor, which in turn shall prevent voltage overshoots and protect the semiconductor against destruction. Therefore it is mandatory to populate a suitable soft-off gate resistor since otherwise the driver cannot turn-off the semiconductor via the soft-off path. A detailed explanation of when the driver is activating the soft-off path is given in chapter 4.8.

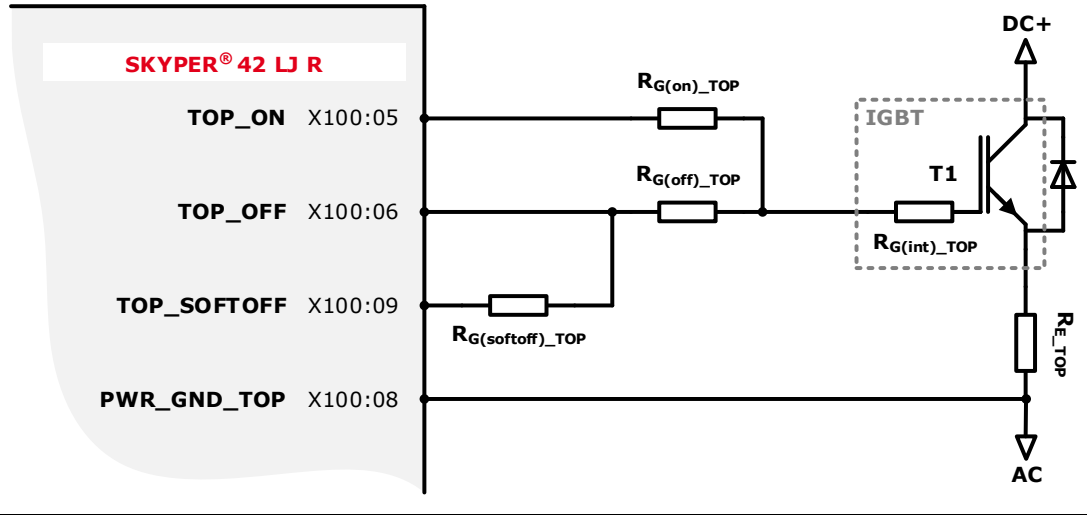
The gate resistor influences the IGBT switching time, switching losses, reverse bias safe operating area (RBSOA), short-circuit safe operating area (SCSOA), EMI, dv/dt, di/dt and reverse recovery current of the freewheeling diode. It has to be selected and optimized very carefully in accordance with the individual application parameters, e.g. IGBT technology, diode, switching frequency, losses, application layout, inductivity / stray inductance, DC-link voltage and driver capability. The complete design of an application must be viewed as a whole, with due considering of the above-mentioned parameters at least. Interactive effects within the whole application must be evaluated and accommodated. [4]

The minimum value of the gate resistors $R_{G(on)}$ and $R_{G(off)}$ could be calculated by the following equation:

$$R_{G(\min)} = R_G + R_{G(int)} + R_E = \frac{V_{G(on)} - V_{G(off)}}{I_{out(peak)}}.$$

The minimum value of the $R_{G(softoff)}$ is 1Ω. Additional hints how to determine the values of the gate resistors are given in [4].

Figure 14: SKYPER® 42 LJ R | Secondary side | Gate resistors



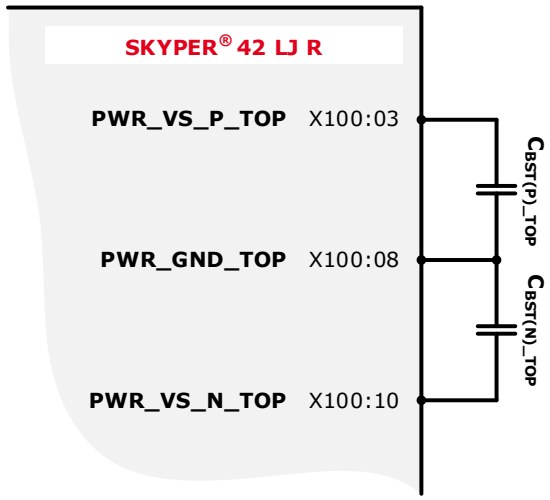
Please note that some of SEMIKRON's driver cores using an ASIC internal N-channel MOSFET for Soft Off. To protect this MOSFET against back swings when turning-off the TOP_ON/BOT_ON channel it is recommended to place the $R_{G(softoff)}$ resistor in series to the $R_{G(off)}$ resistor.
Since each turn-on and turn-off of a semiconductor means charging or discharging the parasitic input capacitance of the semiconductor, the gate resistor has to be pulse load proofed. For this reason SEMIKORN recommends the use of following resistors.

Description	Shape	Manufacturer	Art. no.
MELF resistors	MELF / MiniMELF SMD	Vishay Beyschlag, Vishay Draloric, Vitrohm	PRO MELF resistors, SMM0207, SMM 0204, ZCM series

4.11 External boost capacitors | Secondary side

The SKYPER® 42 LJ R allows driving of semiconductor power modules with a gate charge (Q_G) of up to 20µC per output. To stabilize the gate voltages $V_{G(on)}$ and $V_{G(off)}$ during the semiconductor switches the use of boost capacitors per channel are recommended, if the connected gate charge is larger than 2.5µC. These capacitors has to be placed as close as possible to the driver, as shown in Figure 15.

Figure 15: SKYPER® 42 LJ R | Secondary side | Boost capacitors



The external boost capacitors can be calculated by following equation:

$$C_{BST(P)} = C_{BST(N)} = 4\frac{\mu F}{\mu C} \cdot Q_G - 10\mu F \qquad for\ 2.5\mu C < Q_G \leq 20\mu C$$

Please note, when assembling boost capacitors at the secondary side, also boost capacitors has to be assembled at the primary side, as shown in Figure 9.

$$C_{BST} = C_{BST(P)} = C_{BST(N)}$$

5. Protection features

5.1 Failure management

The SKYPER® 42 LJ R driver core detects several error events on primary and secondary side. The driver's reaction on those events depends on the selected error mode, as described in chapter 4.8. The following table covers all possible error routine scenarios.

Table 7: SKYPER® 42 LJ R | Failure management

Conditions			Reaction		
Error event	**Occurrence**	***CFG_ERR***	***nERR_OUT***	**Outputs**	**Turn-off path**
Undervoltage of power supply	primary side	HIGH/LOW	LOW immediately	OFF and locked, immediately, until reset	Standard
nERR_IN at low-level	primary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Standard
		LOW	LOW immediately	OFF and locked, immediately, until reset	Standard
Undervoltage of power supply	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	
Short circuit detection (DSCP)	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	
nERR_IN at low-level	secondary side	HIGH	LOW immediately	OFF, with next turn-off signal at the corresponding input Locked immediately OFF & locked until reset	Soft Off affected channel Standard not affected channel
		LOW	LOW immediately	OFF and locked, immediately, until reset	

If the SKYPER® 42 LJ R driver has entered the error state, it must be reset before it can resume operation again. The driver could be reset under the following conditions:

- >30µs non-error condition (Reaction on customer side has to be done within that time)
- >9µs no input signals at *TOP_IN/BOT_IN* (Customer confirms error)

After completing the reset sequence the driver returns 'ready for operation' by setting the *nERR_OUT* output to high-level.

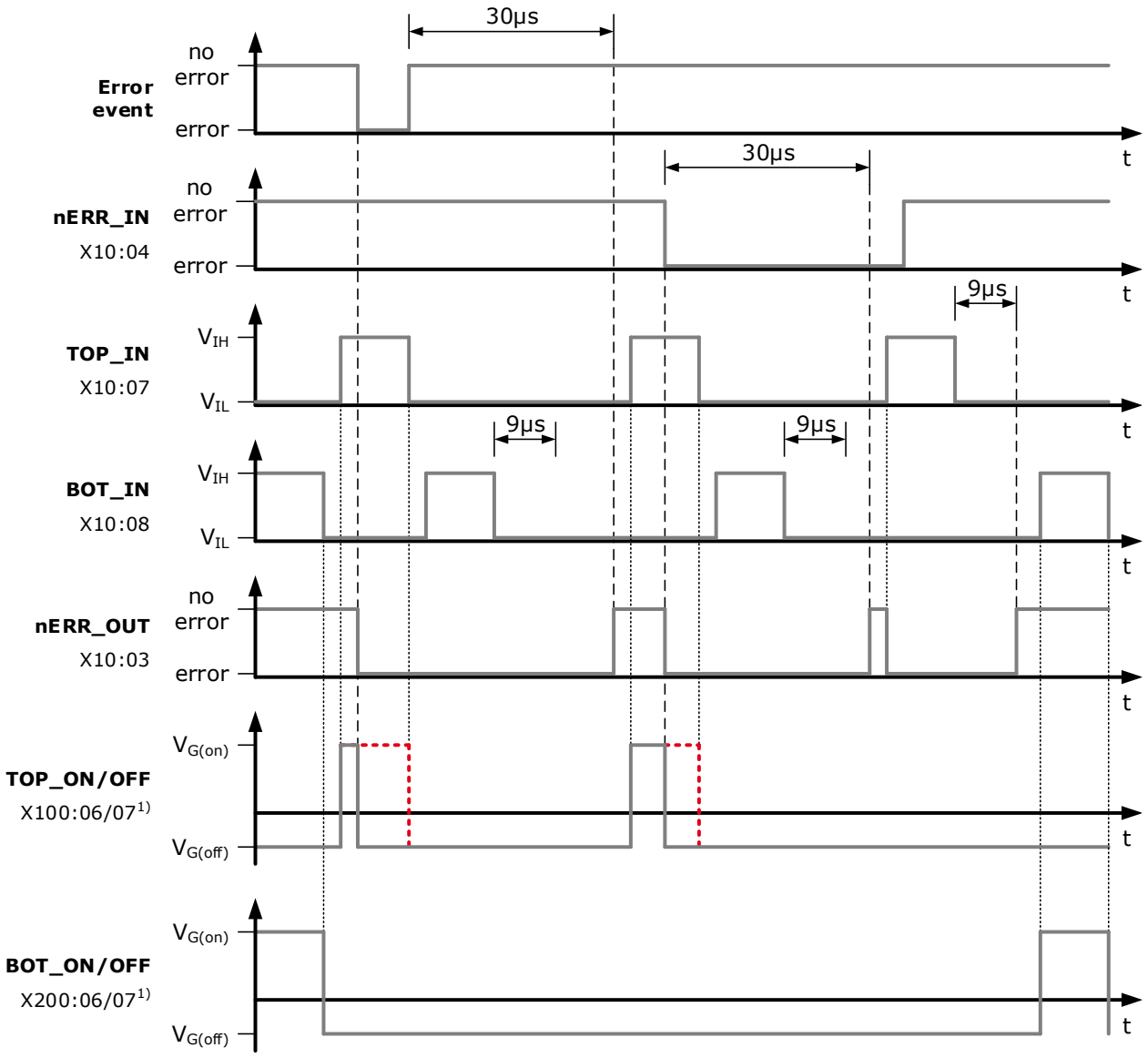
If the driver was entering error state because of an externally reported error event by the controller via the *nERR_IN* pin of the customer interface, the driver can be reset under the following conditions:

- > 30µs have elapsed until the external error event occurred
- > 9µs and no input signals at *TOP_IN/BOT_IN*

Important note
In this particular case the driver is ready for operation again, if the *nERR_OUT* output is set to high-level by the driver and the external error signal is removed. This behaviour prevents deadlock situations, if several drivers are using the bi-directional HALT feature, as described in chapter 4.7.

The behaviour of the driver on an error event is also shown in Figure 16. The red dotted lines mark the behaviour of the driver, if the error configuration pin *CFG_ERR* is connected to *PWR_VS*.

Figure 16: SKYPER® 42 LJ R | Behaviour on error event



1) The signal characteristics of BOT_ON/OFF and TOP_ON/OFF are valid if the outputs X100:06 and X100:07 respectively the outputs X200:06 and X200:07 are connected to each other through the gate resistors.

5.2 Dead time and Interlock

The internal dead time generation of the SKYPER® 42 LJ R as well as the interlock feature can be selected via the configuration pin *CFG_IDT*. The following modes could be selected:

- Interlock enabled, 2µs dead time
- Interlock disabled, no dead time

Interlock enabled

To enable the interlock feature the *CFG_IDT* pin has to be connected to *PWR_GND*. The interlock feature is typically used when driving power semiconductor modules in half bridge configuration. The feature prevents the two outputs from being activated simultaneously which would lead to shorted DC-link (bridge shoot through). The interlock feature allows controlling a power semiconductor module with one switching signal and its inverted signal at the driver's inputs *TOP_IN/BOT_IN*.

The internal timer which generates the dead time, starts with each turn-off command at the inputs *TOP_IN/BOT_IN*. As long as the dead time of 2µs has not been elapsed the driver locks the other output. If the pulse pattern generated by the customer's controller also includes a dead time, the resulting system dead time will be determined by either the controller or the driver, depending on whichever dead time is longer. The SKYPER® 42 LJ R does not add the internal generated dead time to the dead time of the pulse pattern of the controller.

Interlock disabled

When the interlock feature is disabled by connecting the configuration pin *CFG_IDT* to the *PWR_VS* pin both outputs of the driver can be switched independently from each other. Both output channels could be switched-on at the same time.

Table 8 shows the resulting system dead time depending on the configuration via the *CFG_IDT* pin.

Table 8: SKYPER® 42 LJ R | Resulting system dead time

CFG_IDT	Interlock	Controller dead time	SKYPER dead time	Resulting dead time
LOW	Enabled	No dead time	2µs	2µs
LOW	Enabled	< 2µs	2µs	2µs
LOW	Enabled	> 2µs	2µs	>2µs
HIGH	Disabled	2µs	No dead time	2µs
HIGH	Disabled	No dead time	No dead time	No dead time

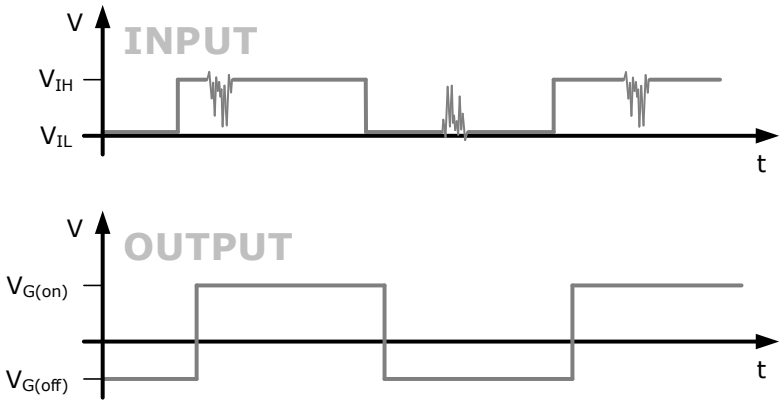
Important Note

When the interlock function is disabled a bridge shoot through has to be prevented by the customer's control unit.

5.3 Short pulse suppression (SPS)

The SKYPER® 42 LJ R driver supresses short on- and off-pulses on the signal inputs *TOP_IN/BOT_IN* and, hence, enhances the interferences ruggedness. The time of suppression corresponds to the filter time set by the customer via the configuration pin *CFG_FLT*, as described in chapter 4.5.

Figure 17: SKYPER® 42 LJ R | Short Pules Suppression



5.4 Undervoltage lockout (UVLO)

The supply voltage of the primary side as well as both positive and both negative gate voltages of the secondary sides are permanently monitored by the driver. If either the supply voltage or a positive gate voltage drops below the 'shutdown' threshold levels the driver enters into error state. The same applies when a negative gate voltage exceeds the 'shutdown' threshold level. Entered into error state the driver executes its error routine as described in chapter 5.1.
The error condition is no longer present, when the supply voltage and both positive gate voltages have exceeded the 'non-error' threshold level and both negative gate voltages have dropped below the 'non-error' threshold level. The driver will be ready again for operation after reset, as described in chapter 5.1

Parameter	Min	Typ	Max
Primary side shutdown threshold	11.6V		
Primary side non-error threshold			13.1V
Secondary side shutdown threshold, positive gate voltage	9.4V		
Secondary side non-error threshold, positive gate voltage			13.3V
Secondary side shutdown threshold, negative gate voltage			-4.1V
Secondary side non-error threshold, negative gate voltage	-5.8V		

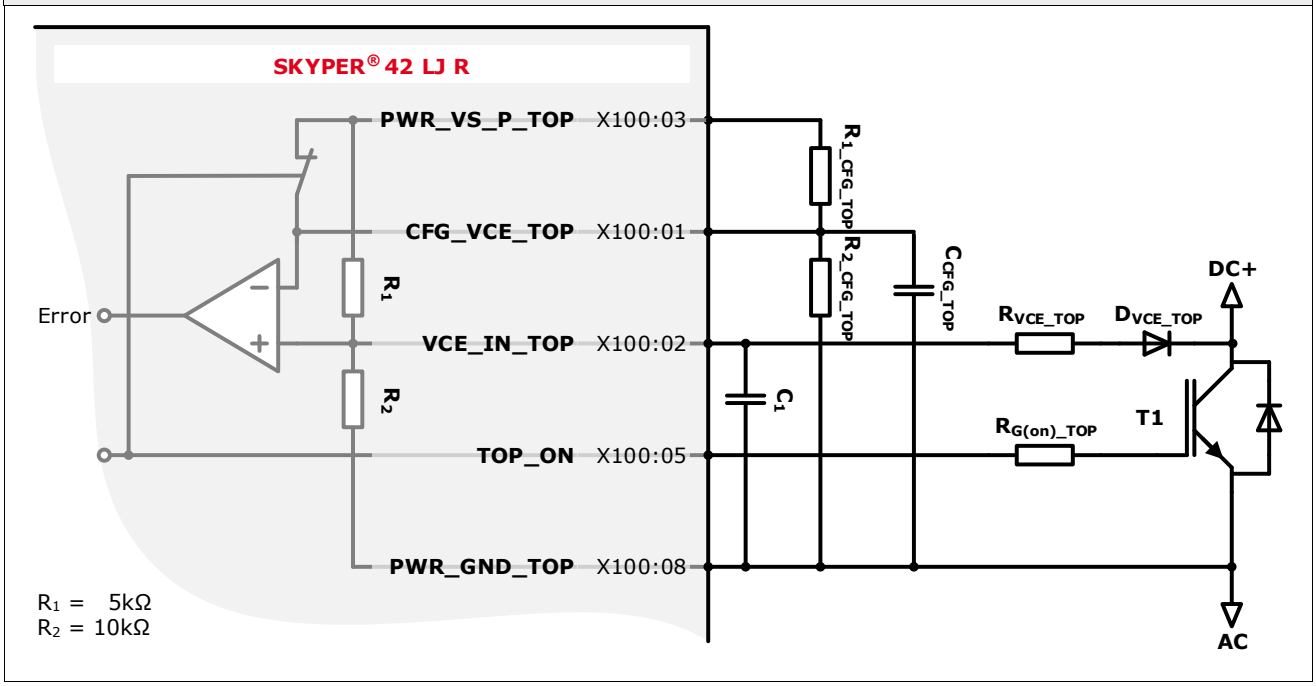
5.5 Dynamic short circuit protection by V_{CEsat}-monitoring (DSCP)

The dynamic short circuit protection feature monitors the collector-emitter voltage V_{CE} of the semiconductor during on-state. When the feature is enabled and the voltage at the *VCE_IN* input exceeds the voltage reference level at the *CFG_VCE* input the driver will enter into error state and will execute its error routine as described in chapter 5.1.

The DSCP feature can be disabled by connecting the *CFG_VCE* pin to the *PWR_VS_P* pin and the *VCE_IN* pin to the *PWR_GND* pin.

Important note
The DSCP feature is designed to detect short circuit conditions and forces the driver react on the desaturation event of a semiconductor. It is not designed for any kind of application over current detection. SEMIKRON recommends to set the DSCP trip level to value of 7V to 9V (voltage at the *CFG_VCE* pin) to prevent unwanted accidently triggered desaturation events due to a too small gap between the saturation voltage of the IGBT and the trigger level of the DSCP feature.

Figure 18: SKYPER® 42 LJ R | Recommended DSCP circuitry



Recommended values		
Component	**Value**	**Remark**
C_1	≤1nF	Optional filter capacitors suppressing high-frequency interfering signals.
C_{CFG}	-	Dimensioning according to chapter 5.5.2
D_{VCE}	-	- The diode must block V_{CEmax}, when the IGBT switches off - The diode must provide functional insulation - Revers recovery charge of the diode causes additional pulse loads at R_{VCE}
R_{1_CFG}	~30kΩ	Dimensioning according to chapter 5.5.2
R_{2_CFG}	-	Dimensioning according to chapter 5.5.2
$R_{G(on)}$	-	Dimensioning according to chapter 4.10
R_{VCE}	511Ω	Resistor should be surge proof

5.5.1 DSCP | Functional description

As long as the driver keeps the semiconductor in off-state the high voltage diode D_{VCE} is operating in reverse direction. The voltage $V_{CE(IN)}$ at the *VCE_IN* pin is set to 10V by the voltage divider of R_1 and R_2. The *CFG_VCE* pin is internally shorten to *PWR_VS_P* and pulls the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin to *PWR_VS_P*. The output of the internal comparator is forced to its negative rail voltage.

When the driver initiates the turn-on process of the semiconductor the internal bypass will be interrupted and the capacitor C_{CFG} discharges until the voltage level defined by voltage divider of R_{1_CFG} and R_{2_CFG} is reached. The trip level during the on-state of the semiconductor has reached the static level ($V_{CE(ref)} = V_{CE(stat)}$).

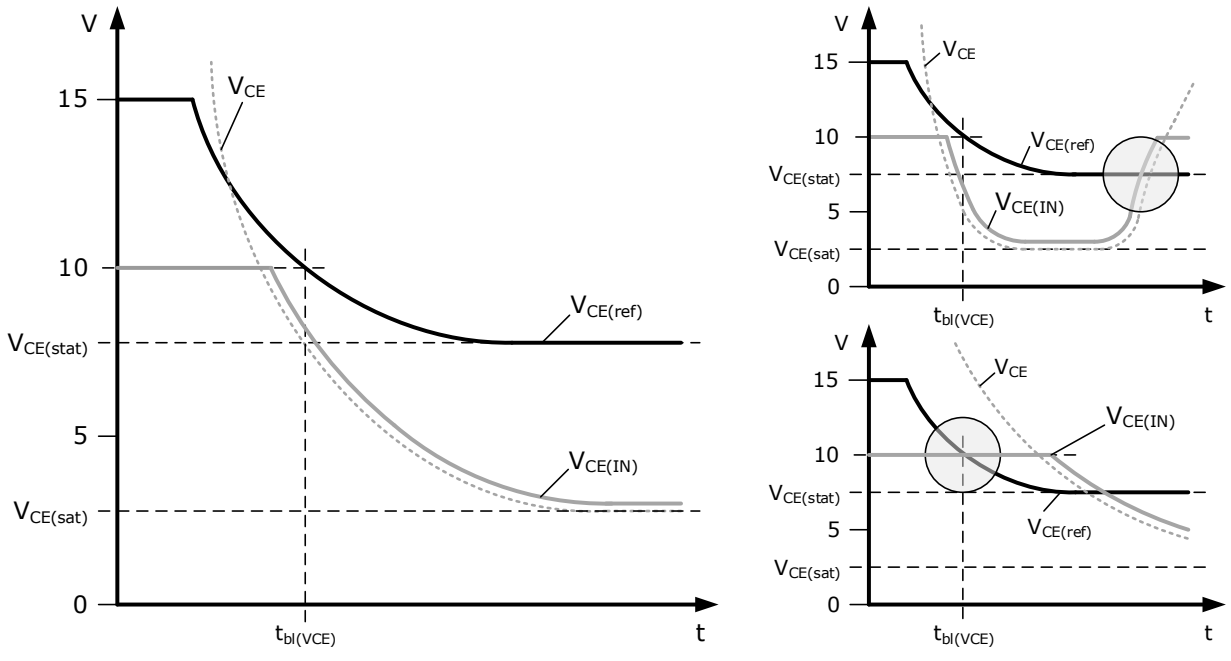
Simultaneously to the discharging process of the capacitor C_{CFG} the semiconductor has to switch into conductive mode and reduces the collector-emitter voltage V_{CE} to V_{CEsat}. When the collector-emitter voltage of the IGBT falls below 10V the high-voltage diode D_{VCE} is starting to operate in forward direction. Now, the voltage $V_{CE(IN)}$ at the *VCE_IN* pin follows the collector-emitter voltage of the semiconductor with an offset caused by the forward current I_F of the high-voltage diode D_{VCE} multiplied by the resistance of R_{VCE} plus the voltage drop V_F of the high-voltage diode.

The DSCP feature is active from the moment the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin is below 10V. The time elapsed from initiating the turn-on process of the semiconductor until the DSCP feature is activated is called blanking time $t_{bl(VCE)}$.

In active state the DSCP triggers an error event, if the voltage $V_{CE(IN)}$ at the *VCE_IN* pin exceeds the voltage $V_{CE(ref)}$ of the *CFG_VCE* pin.

Figure 19 shows on the left side the above described process for a well-configured blanking time $t_{bl(VCE)}$ and static threshold voltage $V_{CE(stat)}$.
The upper right side of Figure 19 shows a desaturation event of an IGBT during the DSCP feature is active. In the moment when the voltage $V_{CE(IN)}$ exceeds the threshold voltage $V_{CE(ref)}$ the driver enters into error state.
Also the lower right side shows an error condition. In this case caused by a too short determined blanking time. The threshold voltage $V_{CE(ref)}$ has already fallen below 10V before the monitored voltage $V_{CE(IN)}$ is below that level.

Figure 19: SKYPER® 42 LJ R | Dynamic short circuit protection



5.5.2 DSCP | Calculation hints

The relevant parameters of the DSCP feature could be calculated with the following equations:

Equation (1) Calculation of the static trip level $(V_{CE(ref)} = V_{CE(stat)})$

$$V_{CE(stat)} = PWR\_VS\_P \cdot \frac{R_{2\_CFG}}{R_{1\_CFG} + R_{2\_CFG}}$$

Equation (2) Calculation of R_{2_CFG} for a certain value of $V_{CE(stat)}$

$$R_{2\_CFG} = \frac{R_{1\_CFG} \cdot V_{CE(stat)}}{PWR\_VS\_P - V_{CE(stat)}}$$

Equation (3) Calculation of the blanking time $t_{bl(VCE)}$ depending on the values of C_{CFG}; R_{1_CFG}; R_{2_CFG}; $V_{CE(stat)}$

$$t_{bl(VCE)} = -C_{CFG} \cdot \frac{R_{1\_CFG} \cdot R_{2\_CFG}}{R_{1\_CFG} + R_{2\_CFG}} \cdot \ln\left(\frac{\frac{10V}{PWR\_VS\_P} \cdot (R_{1\_CFG} + R_{2\_CFG}) - R_{2\_CFG}}{R_{1\_CFG}}\right)$$

Equation (4) Calculation of the voltage $V_{CE(IN)}$ at the *VCE_IN* input depending on the values of V_{CE}; R_{VCE}; V_{D_VCE}

$$V_{CE(IN)} = \frac{R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}} \cdot V_{CE} + \frac{\left(V_{D\_VCE} + \frac{PWR\_VS\_P \cdot R_{VCE}}{R_1}\right) \cdot R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}}$$

5.6 Active clamping

The driver offers the possibility of reducing over voltages during switching by using the active clamping feature. Figure 21 shows an example of an active clamping circuitry based on Zener diodes. The voltage level when the clamping starts is determined by the breakdown voltage of the Zener diodes D_{CLMP}. If, during a switch-off of the IGBT the collector-gate voltage V_{CG} raises beyond the break down voltage V_{Zener} the clamping diodes will get conductive. This leads to a current feeding energy into the gate of the IGBT and switches the IGBT on again, until the V_{CG} voltage is reduced below the V_{Zener} reference.
The *CLMP_IN* input indicates the driver that the collector-gate voltage raised above V_{zener}, if the voltage at the input exceeds the threshold of 13V. When entering active clamping mode the driver sets the output channels to high impedance, which reduces the losses on the driver.

Figure 20: SKYPER® 42 LJ R | Active clamping

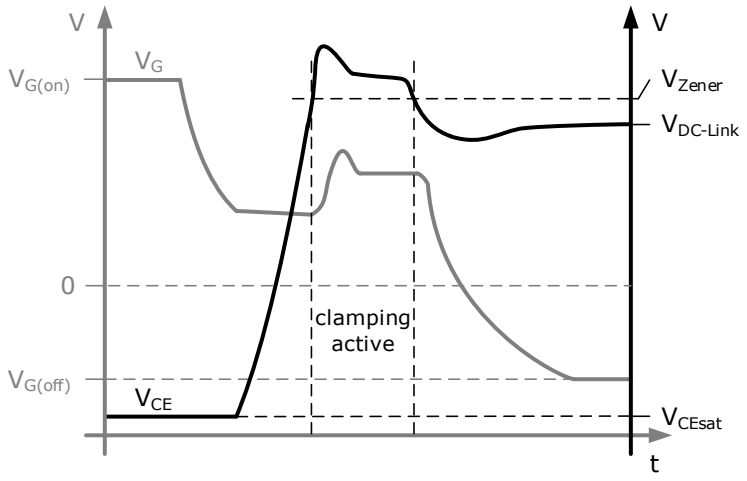
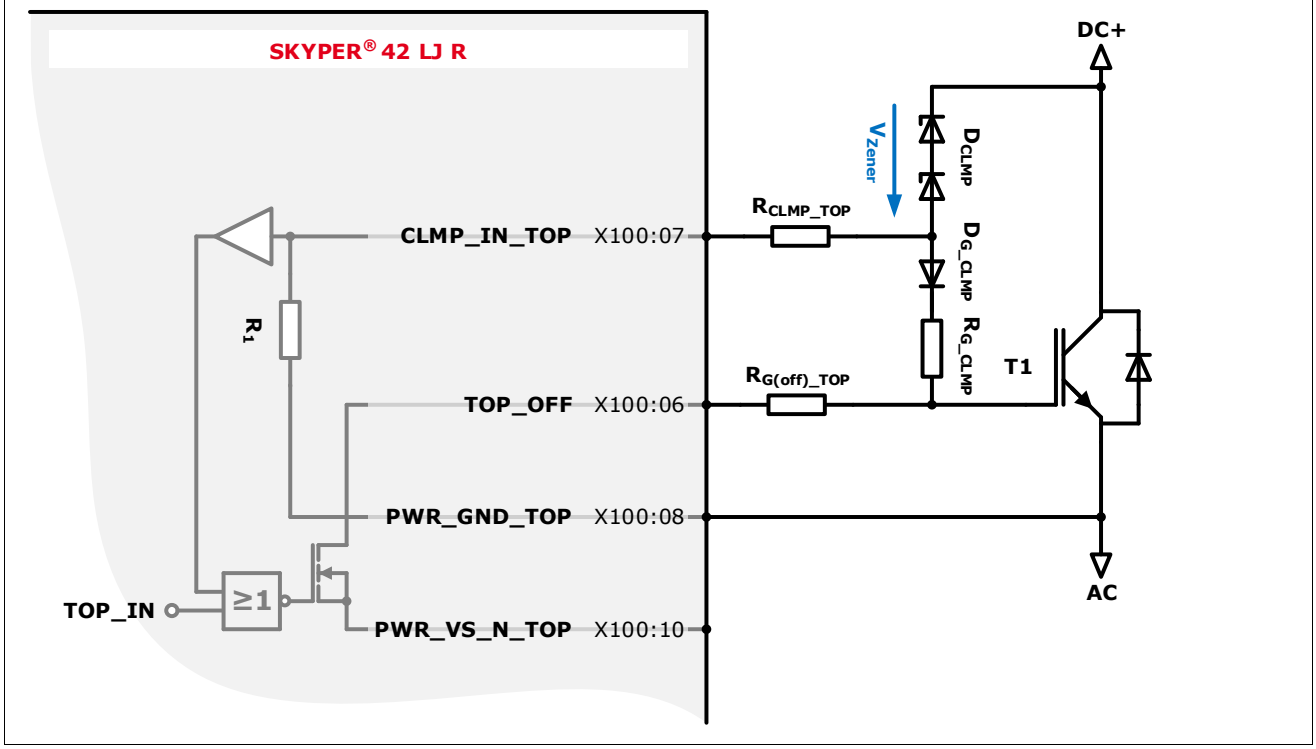


Figure 21: SKYPER® 42 LJ R | Application example for active clamping



Important Note
During the clamping process the IGBT is working in linear mode and generates additional considerable loss. Hence, active clamping must not be operated during standard switching to avoid thermal overstress and reduced IGBT lifetime.

Parameter	Min	Typ	Max
Threshold high CLMP-input	-	-	13 V
Threshold low CLMP-input	2 V	-	-

5.7 Soft Off

The SKYPER® 42 LJ R provides a separate turn-off path *TOP_SOFTOFF/BOT_SOFTOFF* activated by the driver, if an error event is detected on the secondary side, as described in chapter 5.1. Switching-off a semiconductor via the soft-off path aims to reduce the switching speed of the semiconductor and, hence, the over voltage caused by the di/dt through the system's stray inductances is decreased.

Recommendation

Usually the Soft Off resistor is roughly 10 times as high as the standard off resistor. However the proper value has to be very carefully evaluated in the system in accordance with the individual application parameters. Target is to stay within the short circuit proofed time of the IGBT but at the same time reduce the overvoltage below the maximum collector-emitter voltage of the IGBT.

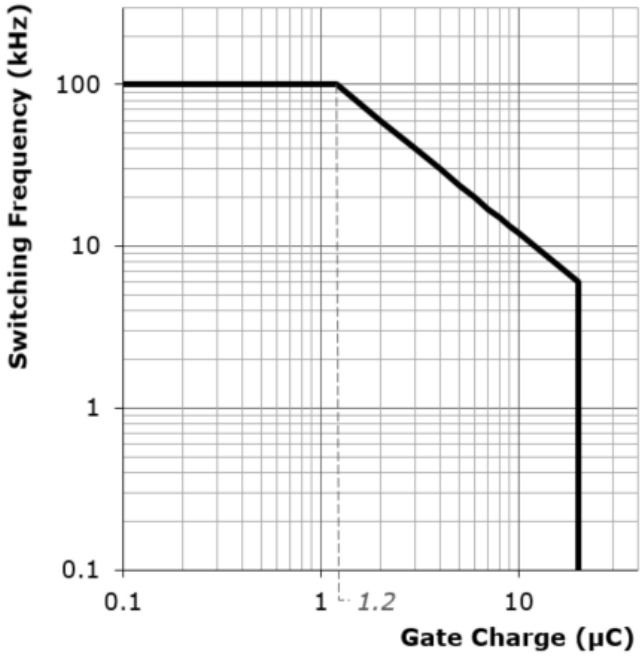
5.8 Safe short circuit turn-off in multilevel topology

Semiconductors in multilevel NPC applications need to be controlled carefully, especially in certain short circuit conditions. A proper turn-off sequence must be maintained to avoid damage to the semiconductors due to over voltage. The integrated DSCP, Soft Off and active clamping features ensures that the SKYPER® 42 LJ R allows the control of the semiconductors in multilevel applications. And thanks to the advanced error management provisions have been taken to allow the application controller to safely handle even short circuit conditions.

Detailed information using the SKYPER® 42 LJ R driver core in multilevel applications can be found in the Application Note AN19-001 "Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies". Thoroughly reading this document is highly recommended before starting tests of multilevel topologies.

6. Electrical characteristic

Figure 22: SKYPER® 42 LJ R | Maximum switching frequency



7. Product Qualification

Table 9: SKYPER® 42 LJ R | Routine tests			
test	**test category**	**test description**	**Standard**
AOI	Automated Opt. Inspection	Control of accurate placement of components/ of solder joints, 100%	SEMIKRON
ICT	In-Circuit Test	Test of the populated PCB, checking the correctly fabrication, 100%	SEMIKRON
FAT	Function Test	Supply current, gate on/off, UVP, error, 100%	SEMIKRON

Table 10: SKYPER® 42 LJ R | Approval tests			
test	**test category**	**test description[1]**	**Standard**
EP	Electrical Parameters	ϑamb = -40°C / +85°C	SEMIKRON
ST	STEP Test	20x 10µs to 2s interruption	EN61000-4-29
ISO	Isolation	4.0 kV AC rms, 60s	EN50178
TC	Thermal Cycling	1000 cycles a 1h, Tstgmax – Tstgmin	IEC60068-2-14
TH	Temperature Humidity	85°C, 85% RH, 1000h	IEC60068-2-67
TS	High/Low Temp Storage	105°C/1000h; -40°C/1000h	IEC60068-2-2/1
BST	Burst	Power terminals: 4kV; Control terminals: 4kV	EN61000-4-4
CC	Climate Change	-15°C to 85°C; 10% to 85%; 10 cycles a 8h	EN60068-2-30
HT	High Temp Operation	95°C, 500h, full load	SEMIKRON
ESD	ESD	Contact discharge: 6kV; Air discharge: 8kV	EN61000-4-2
RFF	Radio Frequency	80 MHz – 2.7GHz, 30 V/m, 80% AM 1kHz	EN61000-4-3
RFD	RF Conducted Disturbance	150 kHz - 80 MHz, 20 V/m, v+h, 80 % AM 1kHz	EN61000-4-6
VB	Vibration	Sinus 20/2000Hz Random 10/2000Hz, 5g, 26 per x,y,z	IEC 60068-2-6
SH	Shock	Half-sinus pulse, 30g, 6000 shocks, 6ms, ±x, ± y, ± z	IEC 60068-2-27

[1] The test conditions are not the maximum applicable conditions for the products. The characteristics of the products are indicated in the data sheet

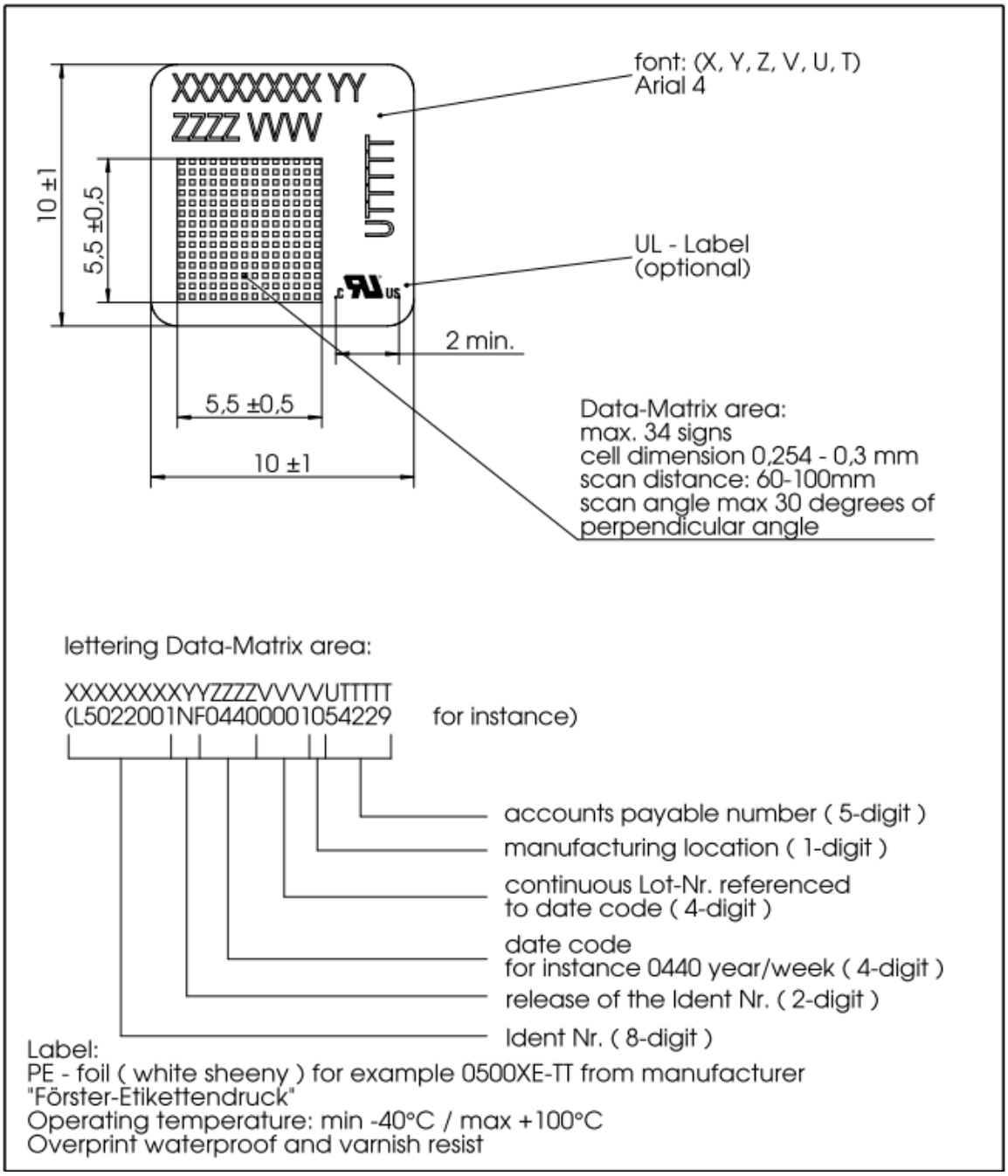
8. Environmental conditions

Table 11: SKYPER® 42 LJ R | Environmental conditions		
Insulation parameters		Rating
Grid voltage		690V
Climatic Classification Pollution Degree (PD)		PD2
Maximum altitude (above sea level)		2000 meter above sea
Overvoltage category (according to EN50178)		OVC 3
Isolation resistance test, Prim-Sec		4000 V AC rms, 60s
Rated insulation voltage (EN60664-1)		8 kV Cat. III
Creepage/clearance distance primary/secondary side		12.2mm
Creepage/clearance distance secondary/secondary side		6.1mm
Climate class		3K3 – IEC 60721-3-3
Environmental Condition	Norm / Standard	
Operating/storage temperature		-40.. +85 °C
High humidity		85 °C, 85%
Flammability	UL94 V0	Heavy flammable materials only
	RoHS / WEEE / China RoHS	
EMC Condition	Norm / Standard	Parameter
ESD	DIN EN 61000-4-2 DIN EN 61800-3	6 kV contact discharge / 8 kV air discharge
Burst	DIN EN 61000-4-4 DIN EN 61800-3	≥ 2kV on adaptor board for signal lines
Immunity against external interference	DIN EN 61000-4-3 DIN EN 61800-3	≥ 30V/m 30MHz – 1000 MHz
Immunity against conducted interference	DIN EN 61000-4-3 DIN EN 61800-3	≥ 20V 150kHz – 80MHz
Shock Vibration		
Vibration	Sinusoidal 20Hz … 500Hz, 5g, 2h per axis (x, y, z) Random 20Hz … 2000Hz, 5g, 2 h per axis (x, y, z)	
Shock	1000 Shocks (6 axis; +-x, +-y, +-z, 1000 shocks per axis), 30g, 18ms Connection between driver and PCB has to be reinforced by support post	

9. Marking

Figure 23: SKYPER® 42 LJ R | Label

Every driver core is marked with a data matrix label. The marking contains the following items.



10. Change history

Revision	Date	Changes
00-01	2011-10-11	Initial draft
02	2012-03-15	Update data sheet, application hints
03	2012-05-15	Differences sample to series
04	2012-09-21	Removal cover, update data sheet, details sample/series
05	2013-09-30	Update primary side ASIC features
06	2014-04-02	Update error management, label
07	2014-07-28	Timing error management
08	2014-09-17	Change to status series release
09	2017-03-07	Update error diagram, Vce values, clamping
10	2017-09-13	Update creepage/clearance
11	2017-10-17	Update handling instruction
12	2019-07-23	Update to new design

References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, “Application Manual Power Semiconductors”, 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3
[3] P. Bhosale, M. Hermwille, AN-7002 “Connection of Gate Drivers to IGBT and Controller”
[4] M. Hermwille, AN-7003 “Gate Resistor – Principles and Applications”
[5] J. Lamp, AN 19-001 “Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies”

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