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# Technical Explanation
# SKYPER®
# 12 PV

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|---|---|
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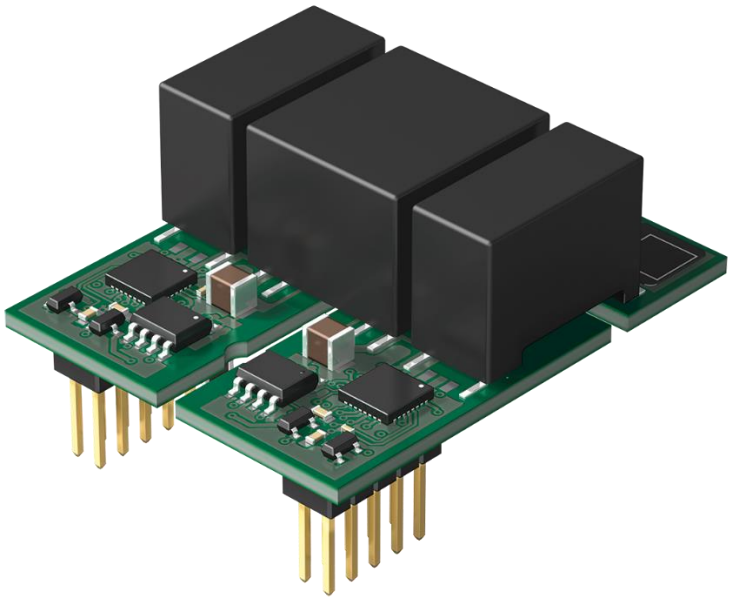
Keyword: IGBT driver core, L5070901

## 1. Introduction

The SKYPER® 12 PV is the most compact driver core within the SKYPER® family and demonstrates its real advantages in low and medium power photovoltaic and ESS applications. In spite of its unrivalled compactness of only 36mm x 45mm the SKYPER® 12 PV provides reinforced insulation for operating voltages of up to 1500 VDC in accordance with EN62109-1 & EN61800-5-1. The powerful output stages of 20A peak current per channel drives semiconductor module with gate charges of up to 20µC reliably. SEMIKRON's highly integrated ASIC technology allows using 30% fewer components than standard solutions which achieve a MTBF rate of 12 million hours at full load for the dual-channel driver core in accordance with the industry standard SN29500.

**Figure 1: SKYPER® 12 PV**



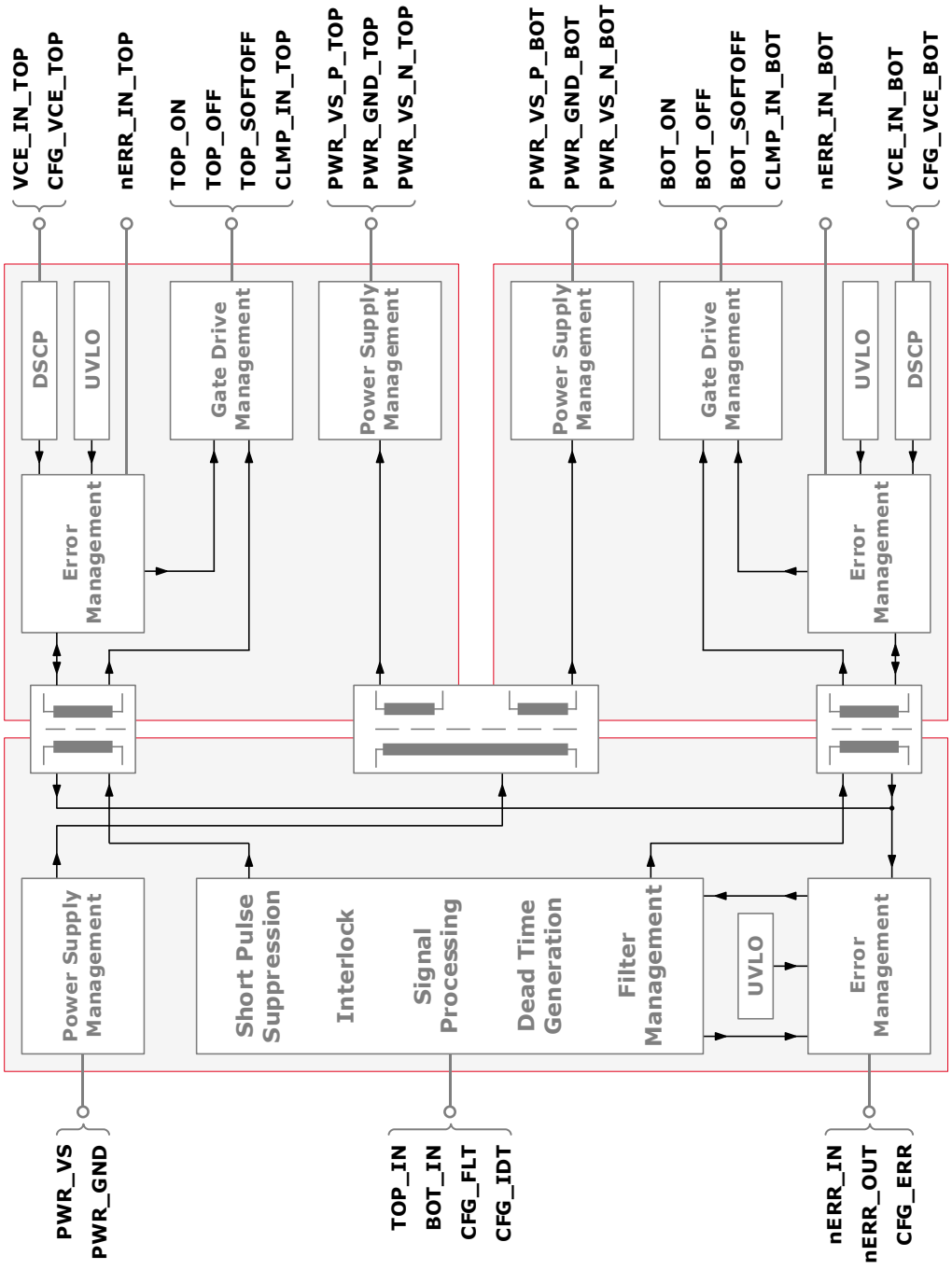
**KEY FEATURES**

- Two output channels
- 1.25W output power and 20A peak output current per channel
- Up to 1500V DC-Link voltage
- ±3 ns jitter per channel
- Fully isolated secondary side power supply
- Selectable filter settings
- Soft turn-off in case of any secondary side error event
- Short pulse suppression (SPS)
- Under voltage lockout (UVLO)
- Dynamic short circuit protection (DSCP)
- Selectable error management modes for standard and multilevel applications
- MTBF rate > 12 Million hours at full load

## 2. Block Diagram and Application Example

### 2.1 Block diagram

**Figure 2: SKYPER® 12 PV | Block diagram**



## 2.2 Application example

Figure 3 and Figure 4 show a typical SKYPER® 12 PV core setup to control a multilevel semiconductor module. The SKYPER® 12 PV employs SEMIKRON's highly-integrated ASIC chipset allowing easy configuration with only a few simple external circuits and in turn reducing the project and development time as well as the cost.

### 2.2.1 Primary side

**Figure 3: SKYPER® 12 PV | Application example | Primary side**

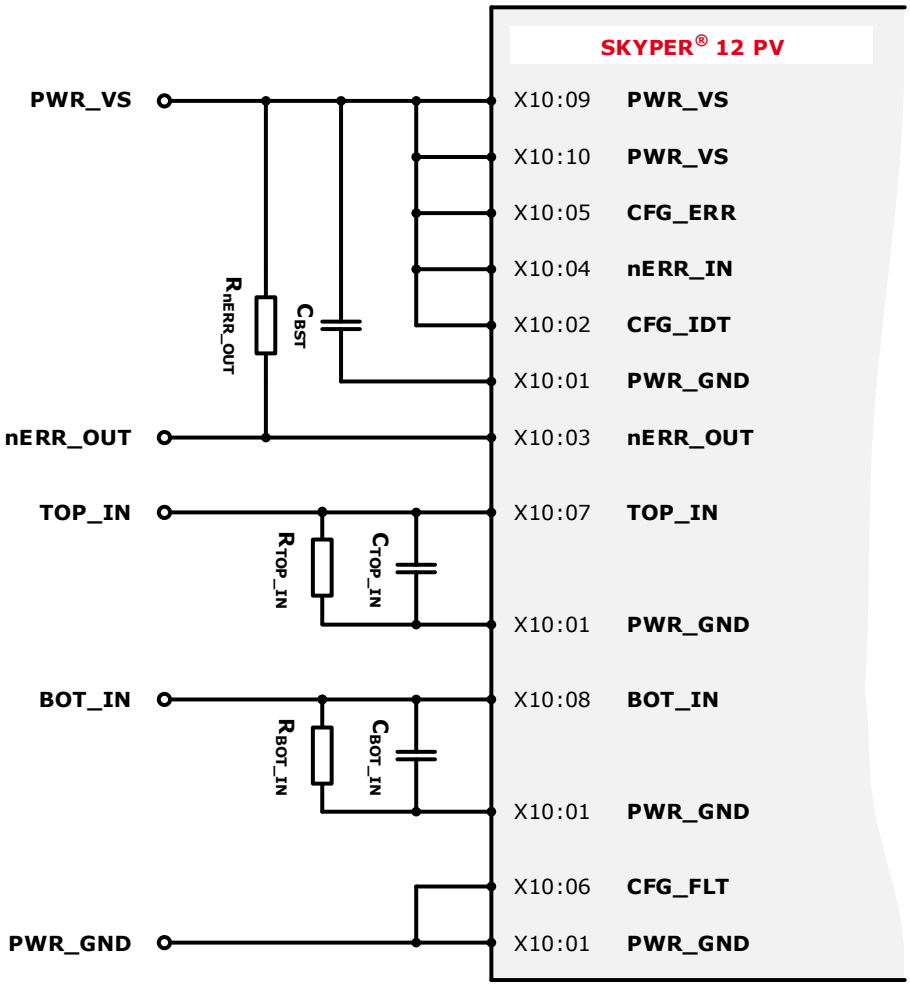
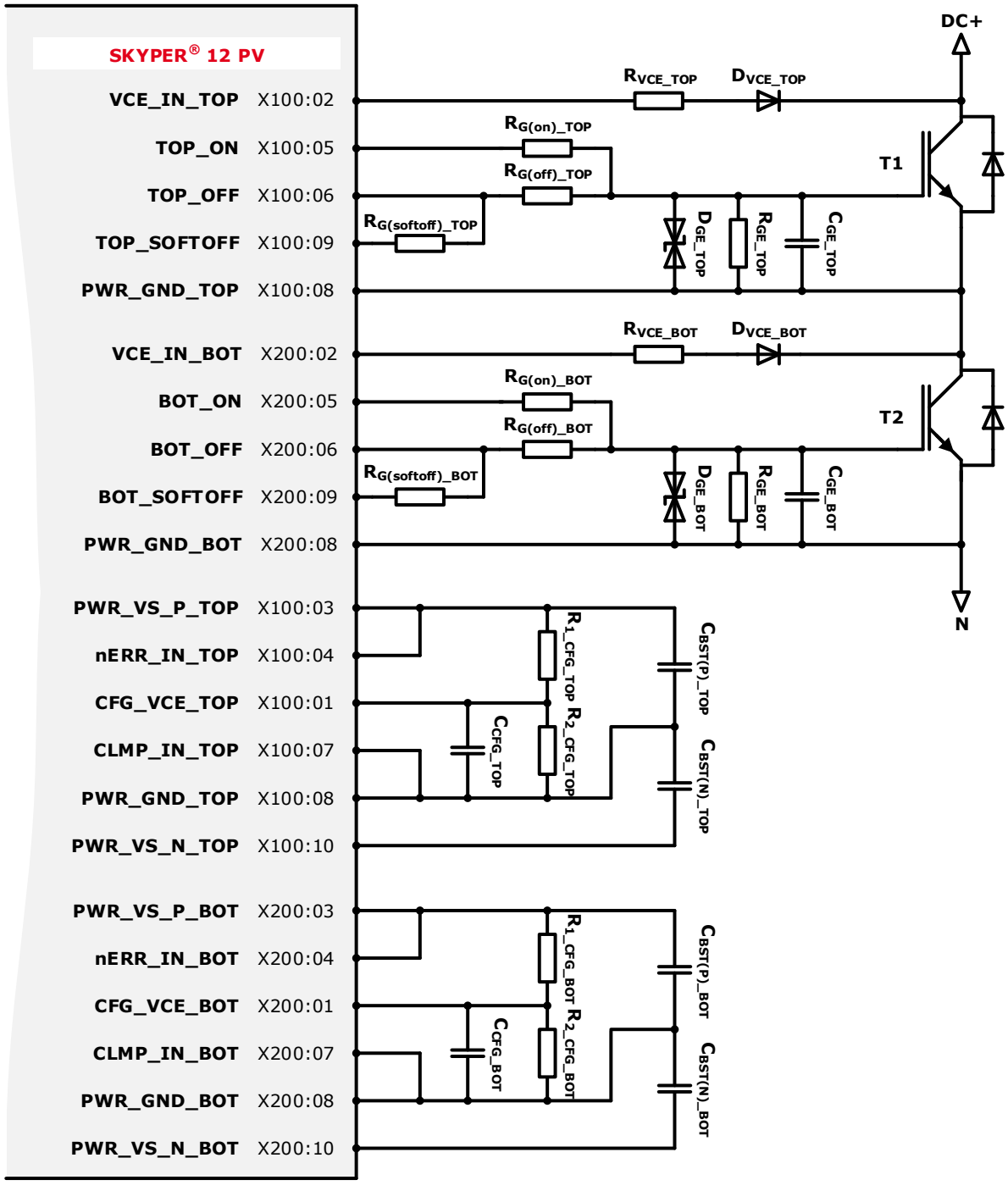



**Table 1: SKYPER® 12 PV | Application example | Primary side | Recommended values**

| Component | Value | Remark |
|---|---|---|
| $C_{TOP\_IN}$ / $C_{BOT\_IN}$ | 1nF | **Optional** filter capacitors suppressing high-frequency signals. For further information please refer to [3]. |
| $C_{BST}$ | - | **Optional** boost capacitor, dimensioning according to chapter 4.11. |
| $R_{TOP\_IN}$ / $R_{BOT\_IN}$ | 10kΩ | **Optional** pull-down resistors, for steady off state of the corresponding output, if no input signal is applied. |
| $R_{nERR\_OUT}$ | 4.75kΩ | **Optional** pull-up resistor, **mandatory** if error output is used. Dimensioning according to chapter 4.6 |

### 2.2.2 Secondary side

**Figure 4: SKYPER® 12 PV | Application example | Secondary side**



| Table 2: SKYPER® 12 PV \| Application example \| Secondary side \| Recommended values | | |
|---|---|---|
| **Component** | **Value** | **Remark** |
| $C_{BST(P)\_TOP}$ / $C_{BST(N)\_TOP}$<br>$C_{BST(P)\_BOT}$ / $C_{BST(N)\_BOT}$ | - | **Optional** boost capacitors, dimensioning according to chapter 4.11. |
| $C_{CFG\_TOP}$ / $C_{CFG\_BOT}$ | - | **Optional** capacitor to adjust the blanking time $t_{bl(VCE)}$ of the dynamic short circuit protection function. **Necessary**, if DSCP is used. Dimensioning according to chapter 5.5. |
| $C_{GE\_TOP}$ / $C_{GE\_BOT}$ | - | **Optional** capacitor to prevent gate oscillation in case of short circuit events or in case of parallel operation of semiconductor power modules. For further information please refer to [3]. |
| $D_{GE\_TOP}$ / $D_{GE\_BOT}$ | $V_{Rmin} \geq V_{G(on)} + 10\%$ | **Optional** suppressor diode to prevent gate voltage overshoots. For further information please refer to [3]. |
| $D_{VCE\_TOP}$ / $D_{VCE\_BOT}$ | - | **Optional** high voltage diode for $V_{CE}$-monitoring, **mandatory** if DSCP is used. Dimensioning according to chapter 5.5. |
| $R_{1\_CFG\_TOP}$ / $R_{1\_CFG\_BOT}$ | ≥ 10kΩ | **Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5. |
| $R_{2\_CFG\_TOP}$ / $R_{2\_CFG\_BOT}$ | - | **Optional** resistors to adjust the trip level $V_{CE(ref)}$ of the dynamic short circuit protection, **necessary** if DCSP is used. Dimensioning according to chapter 5.5. |
| $R_{GE\_TOP}$ / $R_{GE\_BOT}$ | 10kΩ | **Optional** resistor to avoid an open gate of the semiconductor, if the driver is not supplied. For further information refer to [3]. |
| $R_{G(off)\_TOP}$ / $R_{G(off)\_BOT}$<br>$R_{G(on)\_TOP}$ / $R_{G(on)\_BOT}$ | ≥ 1.25Ω | **Necessary** resistors to adjust the semiconductors' turn-on and turn-off behavior. Dimensioning according to chapter 4.10. |
| $R_{G(softoff)\_TOP}$<br>$R_{G(softoff)\_BOT}$ | ≥ 1Ω | **Mandatory** resistor to adjust the semiconductors' turn-off behavior in case of soft turn-off. Dimensioning according to chapter 4.10. |
| $R_{VCE\_TOP}$ / $R_{VCE\_BOT}$ | 511Ω | **Optional** series resistor for $V_{CE}$-monitoring, **mandatory** if DSCP is used. |

Referring to the application example shown in Figure 3 and Figure 4, Table 3 describes the settings made.

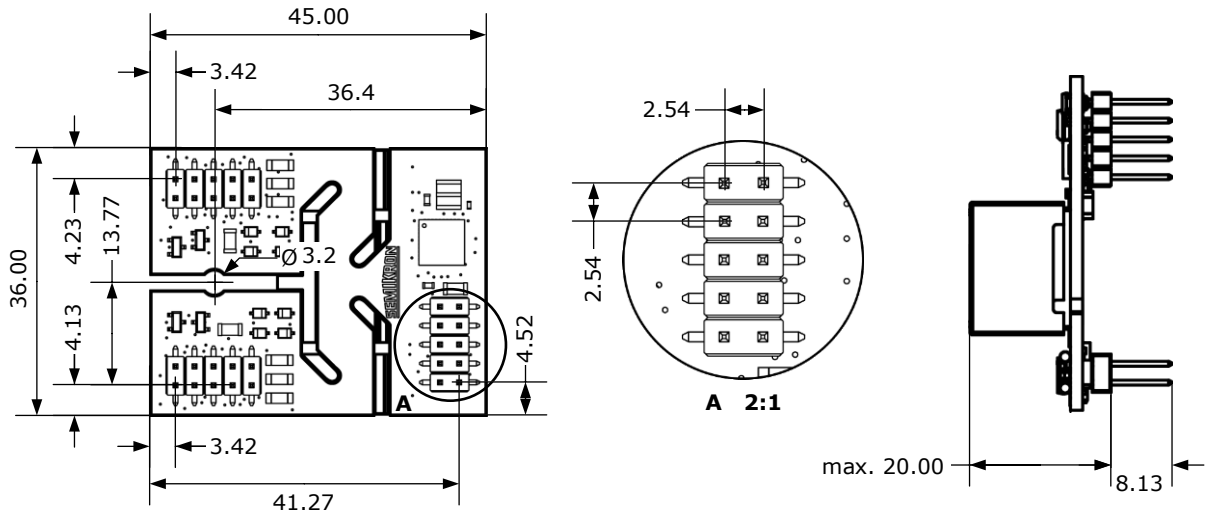
**Table 3: SKYPER® 12 PV | Application example | Settings**

| Function | Configuration | Remark | Chapter |
|---|---|---|---|
| Active clamping | Disabled | Disabled by connecting the pins *CLMP_IN_TOP* and *CLMP_IN_BOT* to the corresponding *PWR_GND* pins. | 5.6 |
| Bidirectional error (=HALT) | Disabled | Disabled by connecting the pin *nERR_IN* to pin *PWR_VS*. | 4.7 |
| Dynamic short circuit protection (DSCP) | Enabled at both output channels | Enabled by connecting the pins *VCE_IN_TOP* and *VCE_IN_BOT* to the corresponding collectors of the semiconductors through $R_{VCE\_TOP}$, $D_{VCE\_TOP}$ and $R_{VCE\_BOT}$, $D_{VCE\_BOT}$. DSCP configuration via pins *CFG_VCE_TOP* and *CFG_VCE_BOT*. | 5.5 |
| Dead time generation | Disabled | Disabled by connecting pin *CFG_IDT* to pin *PWR_VS*. | 5.2 |
| Error mode | In case of any secondary side error condition the event will be reported at the pin *nERR_OUT*. The driver turns-off the affected output immediately and the second output with the next turn-off signal at the corresponding input. Both outputs remain blocked until the error state is reset . | Selected by connecting pin *CFG_ERR* to pin *PWR_VS*. | 5.1 |
| Error propagation delay time | 700ns (typical value) | Fixed value. | 5.1 |
| External error | Disabled at both secondary sides. | Disabled by connecting the pins *nERR_IN_TOP* and *nERR_IN_BOT* to the corresponding *PWR_VS* pins. | 5.1 |
| Filter | Analogue | Selected by connecting pin *CFG_FLT* to pin *PWR_GND*. | 5.3 |
| Interlock | Disabled | Disabled by connecting pin *CFG_IDT* to pin *PWR_VS*. | 5.2 |
| Jitter | ±3ns (typical value) | Selected by connecting the pin *CFG_FLT* to pin *PWR_GND*. | 4.5 |
| Short pulse suppression (SPS) | 200 ns (typical value) | Selected by connecting pin *CFG_FLT* to pin *PWR_GND*. | 5.3 |
| Undervoltage lockout (UVLO) | Always active on primary and secondary side | - | 5.4 |

# 3. Dimensions and mechanical precautions

## 3.1 Dimensions

**Figure 5: SKYPER® 12 PV | Dimension drawing**




All dimensions in mm. Please consider higher tolerances of connector position according to IPC A 610.
STEP file on request.

## 3.2 Plug-in connection

The SKYPER® 12 PV provides simple electrical and mechanical connection to adapter or control boards by its standard pin headers. The primary side and the two secondary side plug-in connectors are 10 pin dual row 2.54mm pin headers. For a secure mechanical connection of the SKYPER 12 PV IGBT driver it is essential that the pin headers can be fully supported by the female mating connectors.

Example for a suitable female mating connector:

| Description | Shape | Manufacturer | Art. no. |
|---|---|---|---|
| (female) RM2.54 10p | SMD 2ROW | Suyin | 254100FA |

Using SMD type mating connectors allows optimized board layout especially for SEMIKRON's spring contact modules like SEMiX.

### 3.3 Support post

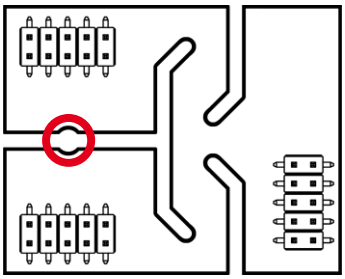
To increase the robustness of the mechanical connection between the SKYPER® 12 PV driver and the corresponding board a support post could be assembled. If a support post is used, make sure it has the correct length. A too short support post would bend both, the driver and the corresponding board that it is mounted on, thus increasing mechanical stress. If the support post is too long, the mating connectors may not fully support the pin header and insufficient or instable electrical and mechanical contact might occur.

The mounting hole is located in the insulation area between the secondary sides of the driver. To avoid reduction of creepage and clearance distances when utilizing a support post, the support post's material must have a CTI 600 classification at least.

Example of a support post:

| Description | Shape | Manufacturer | Art. no. |
|---|---|---|---|
| Nylon support post | Dual lock | Essentra | DLMSPM-8-01 (>12mm) |

**Figure 6: SKYPER® 12 PV | Support post**



mounting hole for support post board

principle of a supported driver on an adapter

### 3.4 Solder connection

The SKYPER® 12 PV driver core can be soldered directly onto an adapter or control board. It should be noted that if the driver is placed too close to the adapter or control board, the clearance distances from the driver's primary to secondary side as well as the clearance distances between the secondary sides may be reduced.

**Soldering hints**

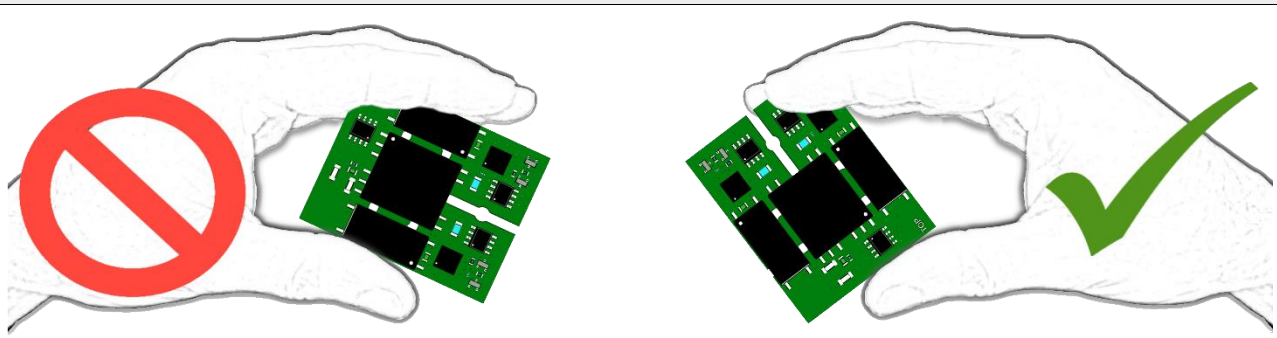
- The solder's temperature must not exceed 260°C and the solder time must not exceed 10 seconds.
- The ambient temperature must not exceed the specified maximum storage temperature of the driver.
- The solder joints should be in accordance to IPC A 610 Revision D (or later) - Class 3 (Acceptability of Electronic Assemblies) to ensure an optimum connection between driver core and printed circuit board.
- The driver is not suited for hot air, reflow or infrared reflow processes.

### 3.5 Handling instructions

Please ensure electric static discharge protection during handling. The driver should only be removed from its original packaging just before mounting. When mounting the driver it has to be ensured that the work is done in an ESD-protected workplace environment. Persons working with the driver have to wear ESD wristbands, overalls and shoes. If tools are used for mounting, those must comply with ESD standards.

When handling the driver, do not pick up the driver at the transformers. The driver MUST be handled at the PCB sides.

**Figure 7: SKYPER® 12 PV | Handling instruction**

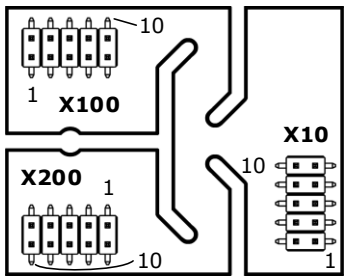


# 4. Interface Description

## 4.1 Footprint

The footprint of the SKYPER® 12 PV with its primary side pin header X10 and the secondary side pin headers X100 and X200 are shown in Figure 8.

**Figure 8: SKYPER® 12 PV | Footprint | Bottom view**




## 4.2 Pin assignment

### 4.2.1 Pin assignment of pin header X10 | Primary side

**Table 4: SKYPER® 12 PV | Pin assignment – Primary side | X10**

| Pin | Signal | Function | Specification |
|---|---|---|---|
| X10:01 | PWR_GND | Ground potential of power supply and digital signals | To be connected to ground |
| X10:02 | CFG_IDT | Interlock dead time configuration | 15V logic; 150kΩ (pull-up)<br>LOW = 2µs interlock dead time<br>HIGH = No interlock dead time |
| X10:03 | nERR_OUT | Error output | Open collector output; max. 18V/15mA (external pull-up resistor needed)<br>LOW = Error<br>HIGH = No error |
| X10:04 | nERR_IN | Error input | 15V logic inverted; 150kΩ/10nF (pull-up)<br>LOW = External error<br>HIGH = No external error |
| X10:05 | CFG_ERR | Error behaviour configuration in case of any error condition | 15V logic; 150kΩ (pull-down)<br>LOW = Both outputs switch off<br>HIGH = Affected output switches off |
| X10:06 | CFG_FLT | Filter configuration for switching signals | 15V logic; 150kΩ (pull-down)<br>LOW = Analogue filter ($t_{SPS(ana)}$)<br>HIGH = Digital filter ($t_{SPS(dig)}$) |
| X10:07 | TOP_IN | Switching signal input (TOP) | 15V logic; 33kΩ/0.01nF (pull-down)<br>LOW = TOP switch off<br>HIGH = TOP switch on |
| X10:08 | BOT_IN | Switching signal input (BOT) | 15V logic; 33kΩ/0.01nF (pull-down)<br>LOW = BOT switch off<br>HIGH = BOT switch on |

| | | | |
|---|---|---|---|
| X10:09 | PWR_VS | Driver power supply | Stabilised +15V ±3% |
| X10:10 | PWR_VS | Driver power supply | Stabilised +15V ±3% |

### 4.2.2 Pin assignment of pin header X100 | Secondary side | TOP

**Table 5: SKYPER® 12 PV | Pin assignment – Secondary side | TOP | X100**

| Pin | Signal | Function | Specification |
|---|---|---|---|
| X100:01 | CFG_VCE_TOP | $V_{CE}$-monitoring reference voltage | External voltage divider needed |
| X100:02 | VCE_IN_TOP | $V_{CE}$-monitoring input | External blocking diode needed |
| X100:03 | PWR_VS_P_TOP | Power supply output, positive voltage | Equal to $V_{G(on)}$ (external buffer capacitors can be optionally connected) |
| X100:04 | nERR_IN_TOP | External error input | 15V logic inverted; 150kΩ/0.01nF (pull-up)<br>LOW = External error<br>HIGH = No external error |
| X100:05 | TOP_ON | On signal terminal for TOP semiconductor | External gate resistor needed (under consideration of $I_{out(avg)}$, $I_{out(peak)}$, $V_{G(on)}$) |
| X100:06 | TOP_OFF | Off signal terminal for TOP semiconductor | External gate resistor needed (under consideration of $-I_{out(avg)}$, $-I_{out(peak)}$, $V_{G(off)}$) |
| X100:07 | CLMP_IN_TOP | $V_{CE}$-clamping input | 150kΩ/0.01nF (pull-down)<br>In case of activated TOP_OFF:<br>LOW = TOP_OFF equal to $V_{G(off)}$<br>HIGH = TOP_OFF floating |
| X100:08 | PWR_GND_TOP | Ground potential of power supply and digital signals | Reference potential of gate voltages (emitter/source of power semiconductor) |
| X100:09 | TOP_SOFTOFF | SoftOff signal terminal for TOP semiconductor | External gate resistor needed |
| X100:10 | PWR_VS_N_TOP | Power supply output, negative voltage | Equal to $V_{G(off)}$ (external buffer capacitors can be optionally connected) |

### 4.2.3 Pin assignment of pin header X200 | Secondary side | BOT

**Table 6: SKYPER® 12 PV | Pin assignment – Secondary side | BOT | X200**

| Pin | Signal | Function | Specification |
|---|---|---|---|
| X200:01 | CFG_VCE_BOT | $V_{CE}$-monitoring reference voltage | External voltage divider needed |
| X200:02 | VCE_IN_BOT | $V_{CE}$-monitoring input | External blocking diode needed |
| X200:03 | PWR_VS_P_BOT | Power supply output, positive voltage | Equal to $V_{G(on)}$ (external buffer capacitors can be optionally connected) |
| X200:04 | nERR_IN_BOT | External error input | 15V logic inverted; 150kΩ/0.01nF (pull-up)<br>LOW = External error<br>HIGH = No external error |
| X200:05 | BOT_ON | On signal terminal for BOT semiconductor | External gate resistor needed (limits under consideration of $I_{out(avg)}$, |

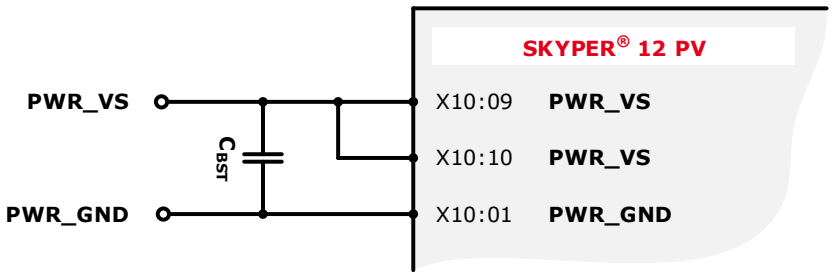
| | | | |
|---|---|---|---|
| | | | $I_{out(peak)}$, $V_{G(on)}$) |
| X200:06 | BOT_OFF | Off signal terminal for BOT semiconductor | External gate resistor needed (limits under consideration of -$I_{out(avg)}$, -$I_{out(peak)}$, $V_{G(off)}$) |
| X200:07 | CLMP_IN_BOT | $V_{CE}$-clamping input | 150kΩ/0.01nF (pull-down)<br>In case of activated BOT_OFF:<br>LOW = BOT_OFF equal to $V_{G(off)}$<br>HIGH = BOT_OFF floating |
| X200:08 | PWR_GND_BOT | Ground potential of power supply and digital signals | Reference potential of gate voltages (emitter/source of power semiconductor) |
| X200:09 | BOT_SOFTOFF | SoftOff signal terminal for BOT semiconductor | External gate resistor needed |
| X200:10 | PWR_VS_N_BOT | Power supply output, negative voltage | Equal to $V_{G(off)}$ (external buffer capacitors can be optionally connected) |

### 4.3 Power supply | Primary side

For a proper operation of the SKYPER® 12 PV driver core, a power supply of at least 15W/1A shall be connected to the driver's power supply pins. During power-up of the driver turn-on signals should not be applied to the driver's inputs *TOP_IN/BOT_IN*, otherwise the driver will not leave the error state.

Please note, when controlling power semiconductor modules with a gate charge ≥ 2.5 µC external boost capacitors ($C_{BST}$) are recommended to support the supply voltage on the primary side. Dimensioning of such boost capacitors shall be done according to chapter 4.11.

**Figure 9: SKYPER® 12 PV | Primary side | Power supply**

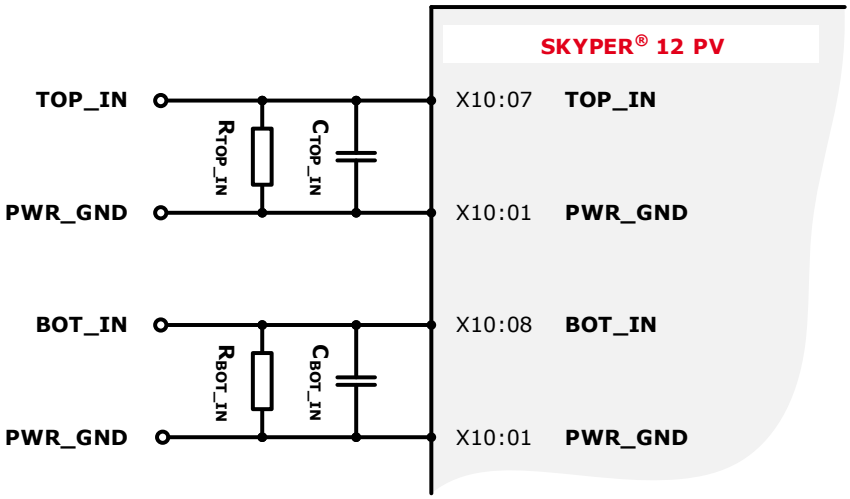


### 4.4 Gate drive signals | Primary side

The signal inputs *TOP_IN/BOT_IN* of the SKYPER® 12 PV driver core have a +15V schmitt trigger logic. A HIGH signal at the input of the driver turns on the corresponding output of the driver. A LOW signal at the input leads to a switch-off command at the corresponding output. Pulses below 1µs are not allowed.

Short pulses as well as voltage peaks, e.g. caused by interference, are suppressed by the driver and will not be transmitted to the outputs. Further information to the short pulse suppression are referred in chapter 5.3.

**Figure 10: SKYPER® 12 PV | Primary side | Gate drive signals**




When using the driver in environments with high levels of electromagnetic noise, it is recommended to connect a filter capacitor ($C_{TOP\_IN}$/$C_{BOT\_IN}$) of several hundred pico Farads as close as possible to the signal inputs. Please note that these capacitors affect the propagation delay time of the driver. The $R_{TOP\_IN}$/$R_{BOT\_IN}$ resistors pull the inputs to low-level when no control signals are applied. The recommended value of the pull-down resistors is approximately 10kΩ.

| Parameter | Min | Typ | Max |
|---|---|---|---|
| Threshold high | - | - | 10V |
| Threshold low | 5V | - | - |

### 4.5 Filter selection, jitter and propagation delay time | Primary side

SEMIKRON's highly-integrated mixed signal ASICs the SKYPER® 12 PV permit the selection of filter type, jitter and propagation delay time to meet specific requirements of applications.

The filter time can be set via the configuration pin *CFG_FLT*. Connecting the *CFG_FLT* pin to the *PWR_VS* pin enables the digital filter employing very low tolerances over the full temperature range.

Depending on the settings made the SKYPER® 12 PV driver provides a very low jitter of typically ±3ns. For this mode, the analogue filter has to be enabled and the driver's internal dead time generator has to be set inactive. The dead time generator is inactive, if either the interlock feature is disabled via the *CFG_IDT* pin or the dead time of the applied pulse pattern is longer than the dead time of internal generator of the driver of typically 2µs. A detailed description of the interlock function and the dead time generation is referred in chapter 5.2.

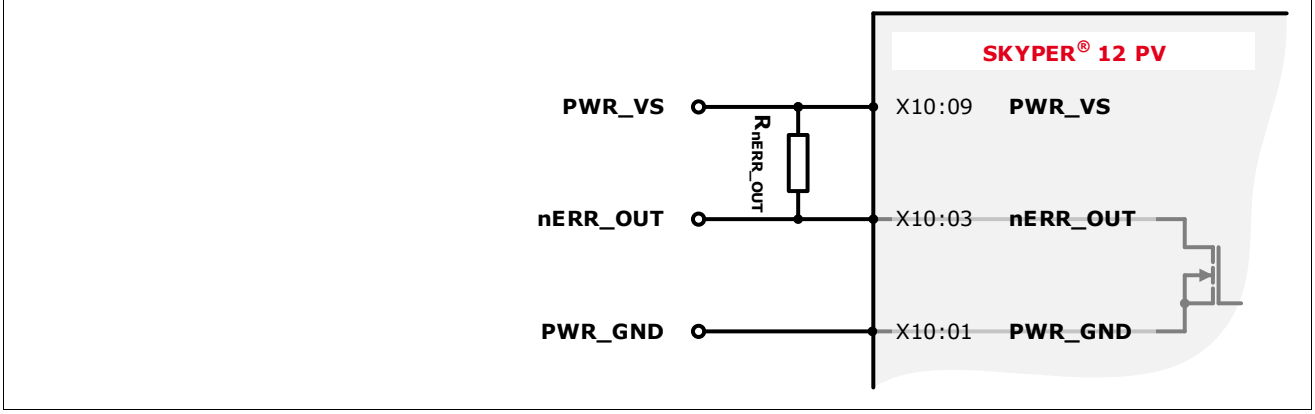
| *CFG_FLT* | *CFG_IDT* | Setting | Filter time | Delay time | Jitter |
|---|---|---|---|---|---|
| HIGH | HIGH/LOW | Digital filter | 390ns | 830ns | ±12.5ns |
| LOW | LOW | Analogue filter | 200ns | 500ns | ±3ns /±12.5ns |
| LOW | HIGH | Analogue filter | 200ns | 500ns | ±3ns |

### 4.6 Error output | Primary side

The SKYPER® 12 PV reports any detected error event at the *nERR_OUT* pin by pulling it to low-level. The error output is an open collector output and requires an external pull-up resistor ($R_{nERR\_OUT}$). The recommended value of the pull-up resistor is in the range of $PWR\_VS/I_{max,nERR\_OUT} \leq R_{nERR\_OUT} \leq 10k\Omega$.
As long as the driver has not been reset the error output will be at low-level.

A detailed description, how to reset the driver to exit the error state and resume to operation is described in chapter 5.1.

**Figure 11: SKYPER® 12 PV | Primary side | Error output**

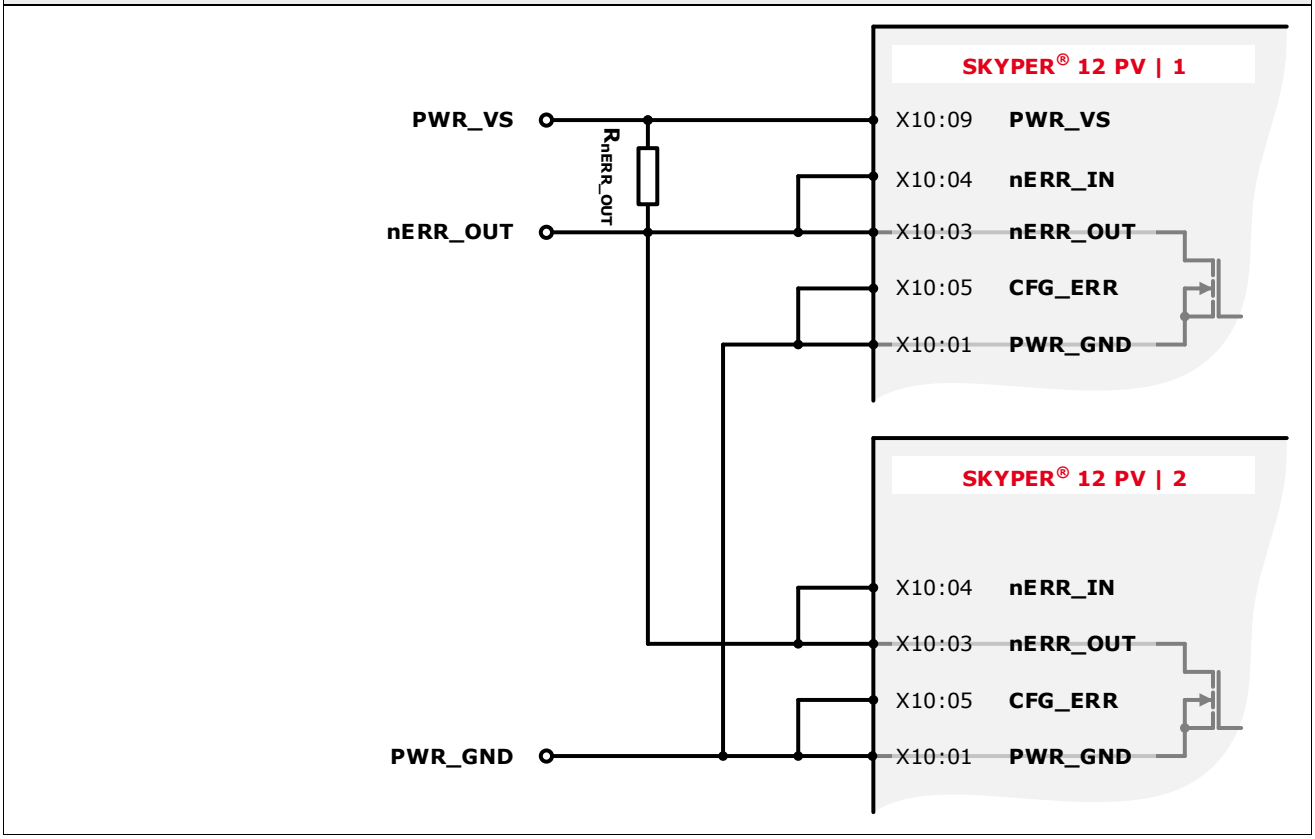



Please note, if the *nERR_OUT* terminal of SKYPER® 12 PV is directly connected to a *nERR_OUT* terminal of another SKYPER® 12 PV driver, only one pull-up resistor must to be applied.

### 4.7 Error input | Primary side

The *nERR_IN* input is optionally used to report a system related external error event to the SKYPER® 12 PV. If the *nERR_IN* input is pulled down to low-level the driver enters into error state. Depending on the error mode configuration, described in chapter 4.8, the driver sets its outputs either immediately or with the next turn-off command at its corresponding input to low-level and locks them. After reset, as described in chapter 5.1, the driver will be ready to transfer the signals to the output stage again. If no reporting to the external error input is required, the *nERR_IN* input can be connected to the *PWR_VS* pin or to the *nERR_OUT* pin.
In multiphase or parallel operation the *nERR_IN* input offers the possibility to force the outputs of each driver in the system to off-state and locks them, simultaneously, without the need of an external control unit. Therefore all *nERR_OUT* outputs and all *nERR_IN* inputs have to be connected together forming a common bi-directional HALT line. Additionally, all *CFG_ERR* configuration pins have to be connected to ground potential, as shown in Figure 12. In this configuration, any driver connected to the HALT line can force the outputs of all connected drivers to off-state and locks them, when the driver pulls its *nERR_OUT* output to low-level.
If a specific turn-off sequence is required – as it is common practice in NPC multilevel applications – the configuration pins *CFG_ERR* have to be connected to the *PWR_VS* pins. A low-level of the HALT line locks the outputs of the connected drivers, but does not immediately force them to low-level. Outputs which are in on-state can be forced to off-state by the controller sending a turn-off command to the corresponding signal inputs *TOP_IN/BOT_IN*.
If the driver is used in environments with high levels of EMI noise, it is recommended to connect an additional filter capacitor as close as possible to the *nERR_IN* pin and the *PWR_GND* pin.

**Figure 12: SKYPER® 12 PV | Primary side | Error input**




| Parameter | Min | Typ | Max |
|---|---|---|---|
| Threshold high | - | - | 11 V |
| Threshold low | 7.5 V | - | - |

### 4.8 Error mode selection | Primary side

The configuration pin *CFG_ERR* selects the behavior of the SKYPER® 12 PV driver core on error events.

Connecting the *CFG_ERR* pin to the *PWR_GND* pin forces the driver to set its outputs to off-state immediately when an error is detected. As long as the driver has not been reset the error event is reported at the corresponding output and the driver's outputs are locked. Whereby, depending on whether an error is detected on the primary or on the secondary side the driver switches off the connected semiconductors via the standard turn-off or the soft-off path. If an error occurs on the primary side the driver will activate the standard turn-off paths of both channels. If an error occurs on the secondary side, the driver will activate the soft-off path of the affected secondary side. The semiconductor connected to the other secondary side will be switched off via the standard turn-off path.

If the *CFG_ERR* pin is connected to the *PWR_VS* pin, the driver locks its outputs in case of any error event's occurrence and, hence, reports the error event at the terminal *nERR_OUT*. The affected output at which the error occurred will be set to off-state, immediately. The second output will be set to off state when the driver has received a turn-off command at the corresponding signal input *TOP_OFF/BOT_OFF*. Depending on whether an error is detected on the primary or secondary side the driver activates the standard turn-off or the soft-off path, as described above.

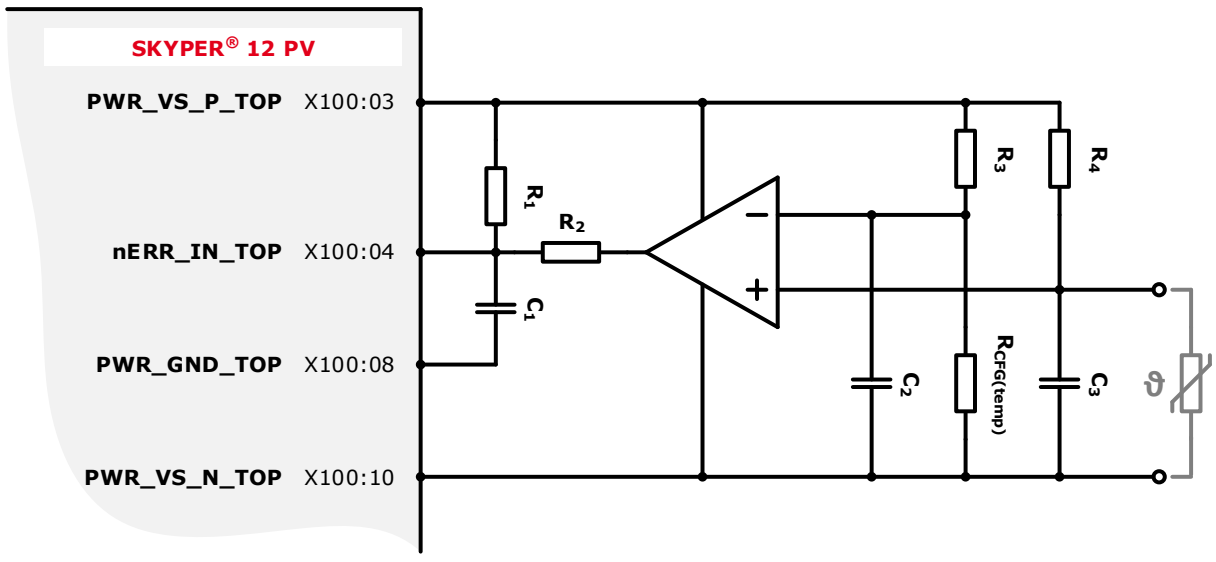
Further information related to the primary and secondary side error events, as well as on the error reset conditions is referred in chapter 5.1.

### 4.9 External error input | Secondary side

Each secondary side of the driver provides an error input (*nERR_IN_TOP/nERR_IN_BOT*) to handle external error events. These inputs are low active. Pulling one input to low-level forces the driver into error state. The behaviour of the driver in case of an external error event depends on the configuration at the configuration pin *CFG_ERR*, as described in chapter 4.8.
The external error input is typically used to monitor temperature, current or voltage of modules, phase legs or systems. The error input of the secondary TOP/BOT side can be disabled by connecting it to the *PWR_VS_P_TOP/PWR_VS_P_BOT* pin.

Figure 13 shows a recommended comparator circuitry to process the NTC's signal and derive the required logic signal for the input of the SKYPER® 12 PV. When the voltage at the comparator's positive input falls below the voltage level of the negative input the *nERR_IN* input will be pulled to low-level and generates an external error event. Assuming that resistors $R_3$ and $R_4$ have the same value the comparator's trip level is reached when the value of the NTC falls below the value of $R_{CGF(temp)}$. Please note that the negative supply pin of the comparator is connected to *PWR_VS_N* which has to be taken into account, in case the NTC thermistor is monitored by an external application circuit in addition.

**Figure 13: SKYPER® 12 PV | Secondary side | Example of an external error input circuitry**



| Recommended values | | |
|---|---|---|
| **Component** | **Value** | **Remark** |
| $C_1$ | 1nF | |
| $C_2$ | 100nF | |
| $C_3$ | 1µF | |
| $R_1$ | 30.1kΩ | |
| $R_2$ | 15kΩ | |
| $R_3$ | 30.1kΩ | |
| $R_4$ | 30.1kΩ | |
| $R_{CFG(temp)}$ | - | The value of the resistor $R_{CFG(temp)}$ has to be determined considering the resistance characteristic of the connected thermistor and the desired trip level. |

| Parameter | Min | Typ | Max |
|---|---|---|---|
| Threshold high | - | - | 13 V |
| Threshold low | 2 V | - | - |

### 4.10 Gate resistors | Secondary side

Equipped with three output channels at each secondary side (*TOP_ON/TOP_OFF/TOP_SOFTOFF* and *BOT_ON/BOT_OFF/BOT_SOFTOFF*) the SKYPER® 12 PV driver offers the possibility to optimize turn-on and turn-off behavior of the IGBT separately. By default, the driver uses the *TOP_ON/TOP_OFF* and *BOT_ON/BOT_OFF* output to turn-on or turn-off the connected semiconductor. The SOFTOFF output will be activated by the driver if a secondary side error event has been detected to turn-off of the connected semiconductor slowly, which in turn shall prevent from excessive voltage overshoots to protect the semiconductor against destruction by over voltage. It is mandatory to populate a suitable soft-off gate resistor, otherwise the semiconductor will not be turned-off in case of a secondary side error. A detailed explanation of when the driver is activating the soft-off path is referred in chapter 4.8.

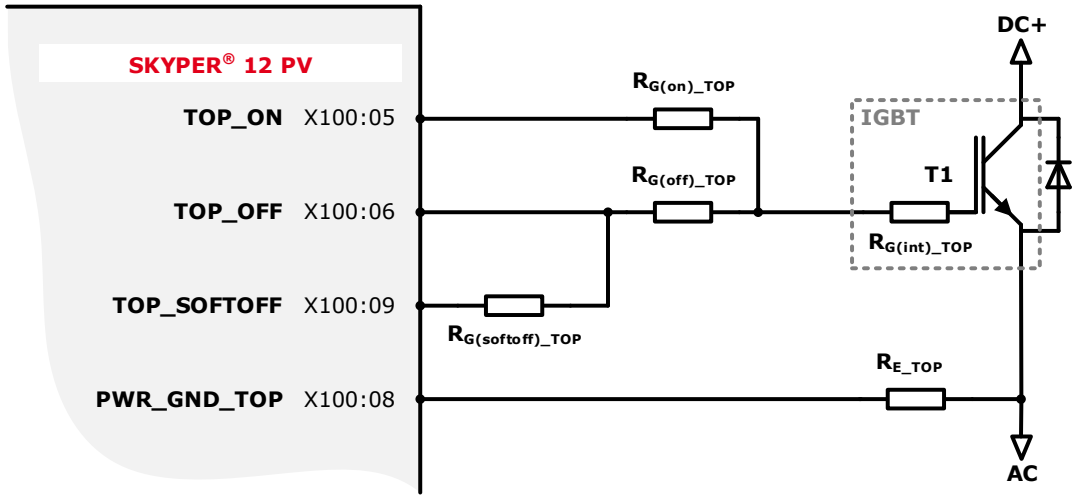
The gate resistor influences the IGBT switching time, switching losses, reverse bias safe operating area (RBSOA), short-circuit safe operating area (SCSOA), EMI, dV/dt, di/dt and reverse recovery current of the freewheeling diode. The gate resistor essentially optimizes the safe operation of the power semiconductor in accordance with the individual application parameters, e.g. IGBT technology, diode, switching frequency, losses, application layout, inductivity / stray inductance, DC-link voltage and driver capability. The complete design of an application must be viewed as a whole, with due considering of the above-mentioned parameters at least. Interacting and interfering effects within the whole application must be considered, evaluated and addressed. [4]

The minimum value of the gate resistors $R_{G(on)}$ and $R_{G(off)}$ could be calculated by the following equation:

$$R_{G(\min)} = R_G + R_{G(int)} + R_E = \frac{V_{G(on)} - V_{G(off)}}{I_{out(peak)}}$$

The minimum allowed value of the $R_{G(softoff)}$ is 1Ω. Additional hints how to determine the values of the gate resistors are referred in [4].

**Figure 14: SKYPER® 12 PV | Secondary side | Gate resistors**



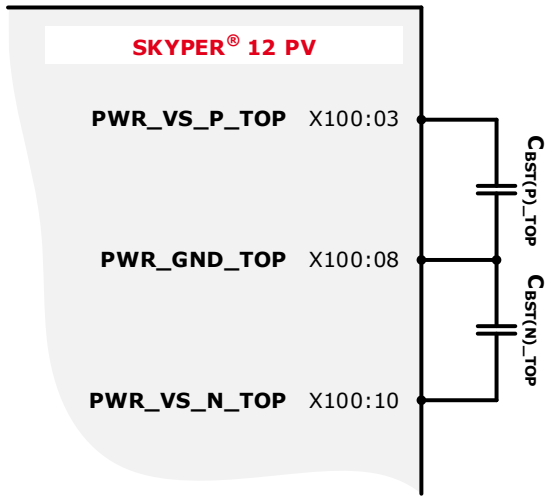

Please note that some of SEMIKRON's driver cores using an ASIC internal N-channel MOSFET for Soft Off. To protect this MOSFET against stress when turning-off the TOP_ON/BOT_ON channel it is recommended to place the $R_{G(softoff)}$ resistor in series with the $R_{G(off)}$ resistor.
Since each turn-on and turn-off of a semiconductor means charging or discharging the input capacitance of the connected power semiconductor, the gate resistor has to be suitable for such pulse load. For this reason, SEMIKRON recommends the use of pulse current suitable resistors. The following table provides examples.

| Description | Shape | Manufacturer | Art. no. |
|---|---|---|---|
| MELF resistors | MELF / MiniMELF SMD | Vishay Beyschlag,<br>Vishay Draloric,<br>Vitrohm | PRO MELF resistors,<br>SMM0207, SMM 0204,<br>ZCM series |

### 4.11 External boost capacitors | Secondary side

The SKYPER® 12 PV allows driving of semiconductor power modules with a gate charge ($Q_G$) of up to 20µC per output. To stabilize the gate voltages $V_{G(on)}$ and $V_{G(off)}$ during the semiconductor switching, the use of boost capacitors for each output channel is recommended, if the connected gate charge is larger than 2.5µC. For maximum effectiveness, these capacitors have to be placed as close as possible to the corresponding terminal as shown in Figure 15.

**Figure 15: SKYPER® 12 PV | Secondary side | Boost capacitors**




The required capacitance of the optional external boost capacitors can be estimated by the following equation:

$$C_{BST(P)} = C_{BST(N)} = A \times Q_G - 4.7\mu F \qquad for\ 2.5\mu C < Q_G \leq 20\mu C$$

$$A = 5 \ldots 7 \frac{\mu F}{\mu C} \qquad IGBT\ 7\ module$$

$$A = 4 \frac{\mu F}{\mu C} \qquad IGBT\ module$$

Please note, when assembling boost capacitors at the secondary sides, also boost capacitors have to be assembled at the primary side, as shown in Figure 9.

$$C_{BST} = C_{BST(P)} = C_{BST(N)}$$

# 5. Protection features

## 5.1 Failure management

The SKYPER® 12 PV driver core detects several different error events on primary and secondary side. The driver's reaction on those events depends on the selected error mode, as described in chapter 4.8. The following table covers the possible error routine scenarios.

**Table 7: SKYPER® 12 PV | Failure management**

| Conditions | | | Reaction | | |
|---|---|---|---|---|---|
| **Error event** | **Occurrence** | ***CFG_ERR*** | ***nERR_OUT*** | **Outputs** | **Turn-off path** |
| Undervoltage of power supply | primary side | HIGH/LOW | LOW<br>immediately | OFF and locked,<br>immediately, until reset | Standard |
| nERR_IN at low-level | primary side | HIGH | LOW<br>immediately | OFF,<br>with next turn-off signal at the corresponding input<br>Locked<br>immediately<br>OFF & locked until reset | Standard |
| | | LOW | LOW<br>immediately | OFF and locked,<br>immediately, until reset | Standard |
| Undervoltage of power supply | secondary side | HIGH | LOW<br>immediately | OFF,<br>affected channel immediately;<br>2nd channel with next turn-off signal at the corresponding input<br>Locked<br>immediately<br>OFF & locked until reset | Soft Off<br>affected channel<br>Standard<br>not affected channel |
| | | LOW | LOW<br>immediately | OFF and locked,<br>immediately, until reset | |
| Short circuit detection (DSCP) | secondary side | HIGH | LOW<br>immediately | OFF,<br>affected channel immediately;<br>2nd channel with next turn-off signal at the corresponding input<br>Locked<br>immediately<br>OFF & locked until reset | Soft Off<br>affected channel<br>Standard<br>not affected channel |
| | | LOW | LOW<br>immediately | OFF and locked,<br>immediately, until reset | |
| nERR_IN at low-level | secondary side | HIGH | LOW<br>immediately | OFF,<br>affected channel immediately;<br>2nd channel with next turn-off signal at the corresponding input<br>Locked<br>immediately<br>OFF & locked until reset | Soft Off<br>affected channel<br>Standard<br>not affected channel |
| | | LOW | LOW<br>immediately | OFF and locked,<br>immediately, until reset | |

If the driver has entered the error state, it must be reset before the driver resumes to operation mode. The driver could be reset under the following conditions:

- >30µs non-error condition (Reaction on customer side should happen within that time)
- >9µs no input signals at *TOP_IN/BOT_IN* (Customer confirms error)

After completing the reset sequence the driver returns 'ready for operation' by setting the *nERR_OUT* output to high-level.

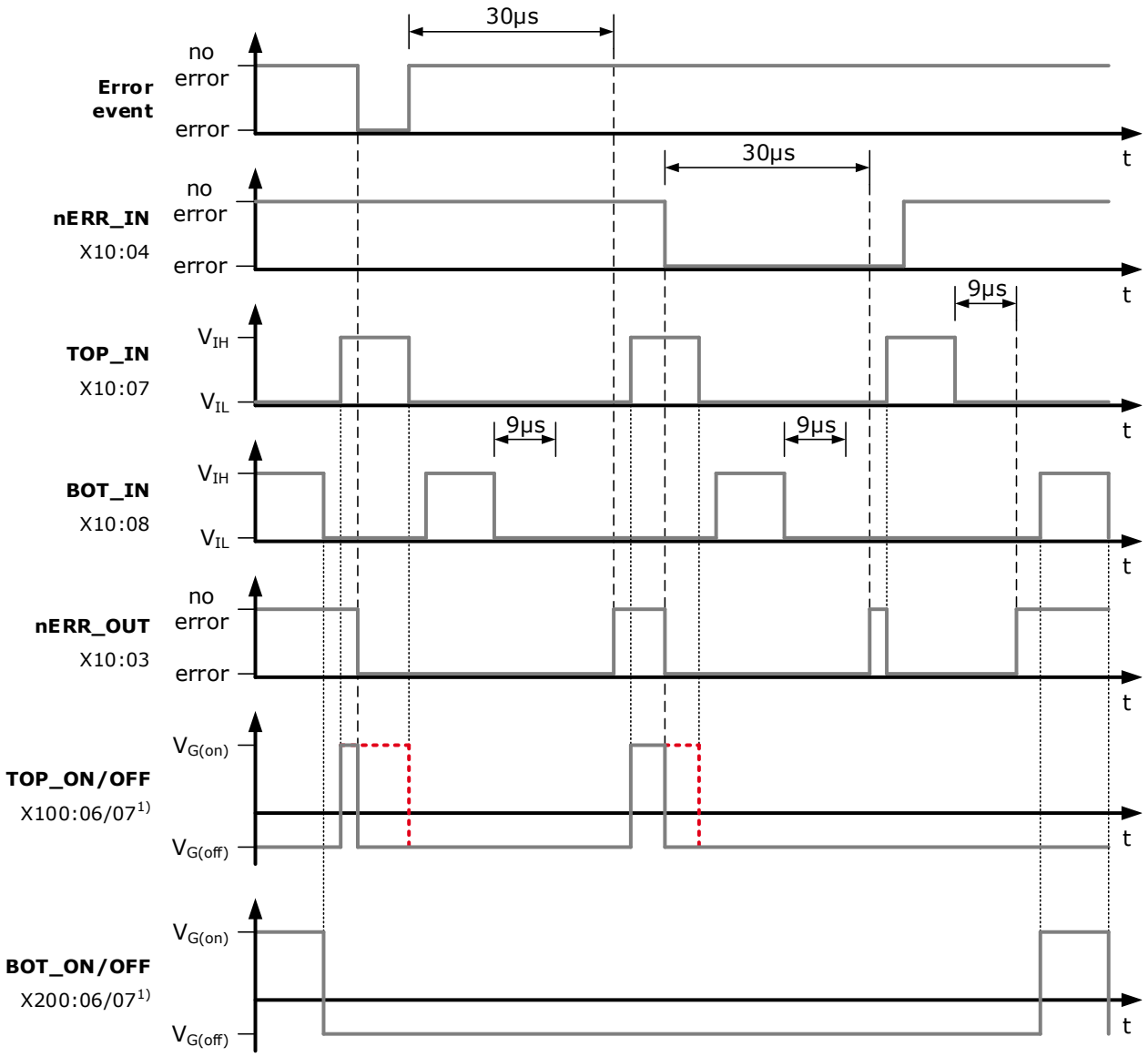
If the driver has entered error state because of an externally reported error event by the controller via the driver's primary side *nERR_IN* pin, the driver can be reset under the following conditions:

- > 30µs has elapsed until the external error event occurred
- > 9µs no input signals at *TOP_IN/BOT_IN*

**Important note**
In this particular case the driver is ready for operation again, if the *nERR_OUT* output is set to high-level by the driver and the external error signal is removed. This behavior prevents deadlock situations, if several drivers are using the bi-directional HALT feature, as described in chapter 4.7.

The behavior of the driver on an error event is also shown in Figure 16. The red dotted lines show the behavior of the driver for the channel for which the error condition was not detected if the error configuration pin CFG_ERR is connected to PWR_VS.

**Figure 16: SKYPER® 12 PV | Behavior on error event**




1) The signal characteristics of BOT_ON/OFF and TOP_ON/OFF are valid if the outputs X100:06 and X100:07 respectively the outputs X200:06 and X200:07 are connected to each other through the gate resistors.

## 5.2 Dead time and Interlock

The internal dead time generation of the SKYPER® 12 PV as well as the interlock feature can be selected via the configuration pin *CFG_IDT*. The following modes are available:

- Interlock enabled, 2µs dead time
- Interlock disabled, no dead time

### Interlock enabled

To enable the interlock feature the *CFG_IDT* pin has to be connected to *PWR_GND*. The interlock feature is typically used when driving power semiconductor modules in half bridge configuration. The feature prevents the two outputs from being activated simultaneously, which would lead to a shorted DC-link connection (bridge shoot through). The interlock feature also allows controlling a power semiconductor module with one switching signal and its inverted signal at the driver's inputs *TOP_IN/BOT_IN*.

The internal timer which generates the dead time, starts with each turn-off command at the inputs *TOP_IN/BOT_IN*. As long as the dead time of 2µs has not elapsed, the driver locks the second output. If the pulse pattern generated by the customer's controller also includes a dead time, the resulting system dead time will be determined by either the controller or the driver, depending on whichever dead time duration is longer. The SKYPER® 12 PV does not add the internal generated dead time to the dead time of the pulse pattern of the controller.

### Interlock disabled

If the interlock feature is disabled by connecting the configuration pin *CFG_IDT* to the *PWR_VS* pin, both outputs of the driver can be switched independently from each other. Hence, both output channels could be switched-on at the same time without blocking.

Table 8 shows the resulting system dead time depending on the configuration via the *CFG_IDT* pin.

**Table 8: SKYPER® 12 PV | Resulting system dead time**

| CFG_IDT | Interlock | Controller dead time | SKYPER dead time | Resulting dead time |
|---|---|---|---|---|
| LOW | Enabled | No dead time | 2µs | 2µs |
| LOW | Enabled | < 2µs | 2µs | 2µs |
| LOW | Enabled | > 2µs | 2µs | > 2µs |
| HIGH | Disabled | 2µs | No dead time | 2µs |
| HIGH | Disabled | No dead time | No dead time | No dead time |

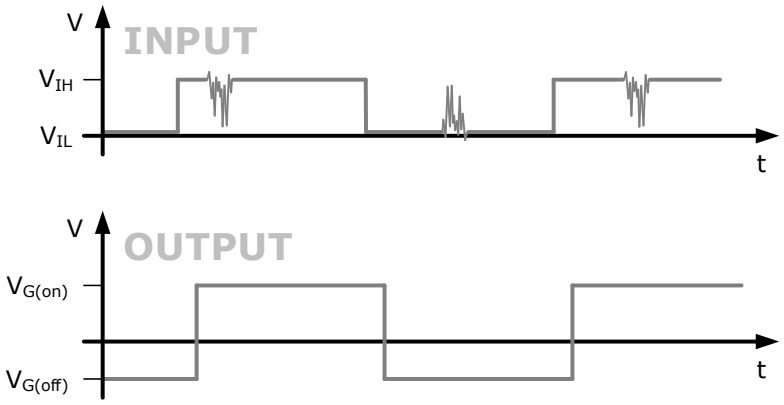
### Important Note

When the interlock function is disabled a bridge shoot through has to be prevented by the user's control unit.

### 5.3 Short pulse suppression (SPS)

The SKYPER® 12 PV driver suppresses short on- and off-pulses at the signal inputs *TOP_IN/BOT_IN* and, hence, enhances the interferences ruggedness. The time of suppression corresponds to the filter time set by the customer via the configuration pin *CFG_FLT*, as described in chapter 4.5.

**Figure 17: SKYPER® 12 PV | Short Pules Suppression**




### 5.4 Undervoltage lockout (UVLO)

The SKYPER® 12 PV driver permanently monitors the supply voltage of the primary side as well as both positive and both negative gate voltages of the secondary sides. If either the supply voltage or a positive gate voltage drops below the 'shutdown' threshold levels the driver enters into error state. The same applies when a negative gate voltage exceeds the 'shutdown' threshold level. Once entered into error state the driver executes its error routine as described in chapter 5.1.
The error condition resets when the supply voltage and both positive gate voltages have exceeded the 'non-error' threshold level and both negative gate voltages have dropped below the 'non-error' threshold level. The driver will be ready again for operation after reset, as described in chapter 5.1

| Parameter | Min | Typ | Max |
|---|---|---|---|
| Primary side shutdown threshold | 12.2V | | |
| Primary side non-error threshold | | | 13.9V |
| Secondary side shutdown threshold, positive gate voltage | 9.4V | | |
| Secondary side non-error threshold, positive gate voltage | | | 13.3V |
| Secondary side shutdown threshold, negative gate voltage | | | -4.1V |
| Secondary side non-error threshold, negative gate voltage | -5.8V | | |

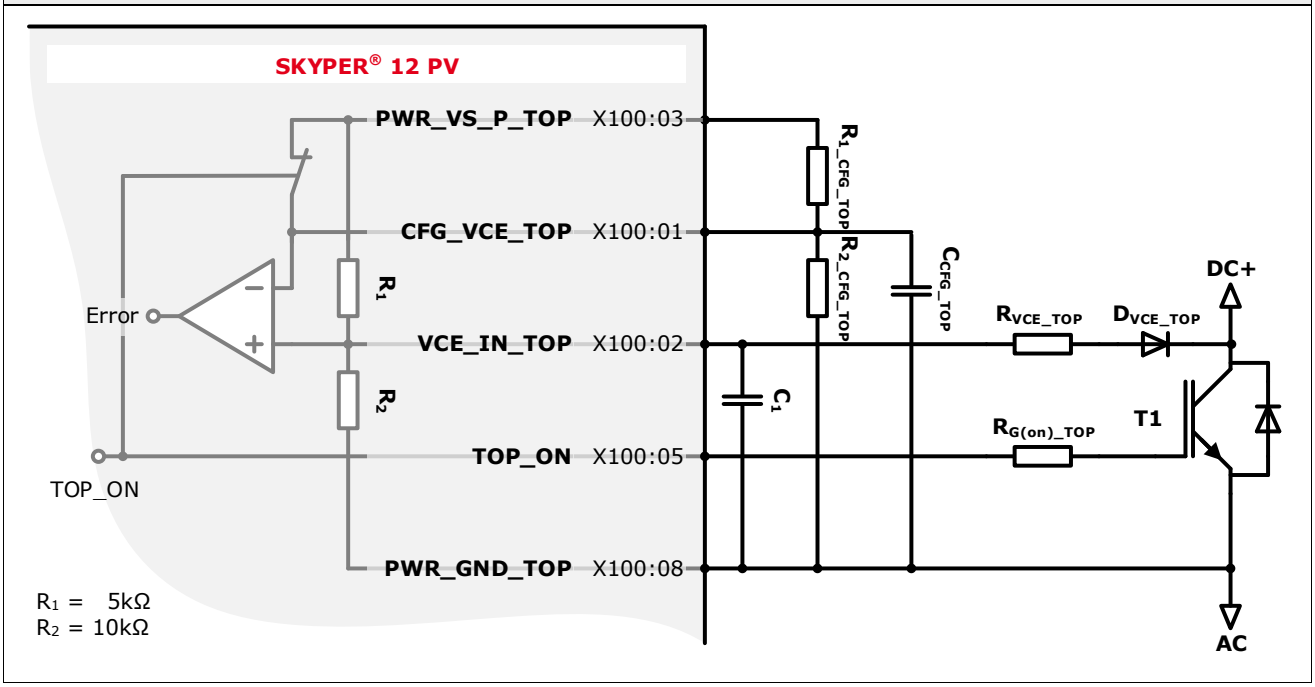
## 5.5 Dynamic short circuit protection by $V_{CEsat}$-monitoring (DSCP)

The dynamic short circuit protection feature monitors the Collector-Emitter voltage $V_{CE}$ of the semiconductor during on-state. When the feature is enabled and the voltage at the *VCE_IN* input exceeds the voltage reference level at the *CFG_VCE* input the driver will enter into error state and will execute its error routine as described in chapter 5.1.

The DSCP feature can be disabled by connecting the *CFG_VCE* pin to the *PWR_VS_P* pin and the *VCE_IN* pin to the *PWR_GND* pin.

**Important note**
The DSCP feature is designed to detect short circuit conditions and forces the driver to react on the desaturation event of a semiconductor. It is explicitly stated that this function is designed to detect short circuit conditions and not to set a specific threshold to detect overcurrent situations e.g. of externally connected applications. SEMIKRON recommends to set the DSCP trip level to a value of 7V to 9V (voltage at the *CFG_VCE* pin) to prevent from unwanted accidently (false) triggered desaturation events due to a too small gap between the saturation voltage of the IGBT and the trigger level of the DSCP feature.

**Figure 18: SKYPER® 12 PV | Recommended DSCP circuitry**



| Recommended values | | |
|---|---|---|
| **Component** | **Value** | **Remark** |
| $C_1$ | ≤1nF | Optional filter capacitors suppressing high-frequency interfering signals. |
| $C_{CFG}$ | - | Dimensioning according to chapter 5.5.2 |
| $D_{VCE}$ | - | - The diode must block $V_{CEmax}$, when the IGBT switches off<br>- The diode must provide functional insulation<br>- Revers recovery charge of the diode causes additional pulse loads at $R_{VCE}$ |
| $R_{1\_CFG}$ | ~30kΩ | Dimensioning according to chapter 5.5.2 |
| $R_{2\_CFG}$ | - | Dimensioning according to chapter 5.5.2 |
| $R_{G(on)}$ | - | Dimensioning according to chapter 4.10 |
| $R_{VCE}$ | 511Ω | Resistor should be surge proof |

### 5.5.1 DSCP | Functional description

As long as the driver keeps the connected semiconductor in off-state the high voltage diode $D_{VCE}$ is operating in reverse direction. The voltage $V_{CE(IN)}$ at the *VCE_IN* pin is set to 10V by the voltage divider of $R_1$ and $R_2$. The *CFG_VCE* pin is internally shorten to *PWR_VS_P* and pulls the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin to *PWR_VS_P*. Hence, the output of the internal comparator is forced to its negative rail voltage.

When the driver initiates the turn-on process of the semiconductor the internal bypass will be interrupted and the capacitor $C_{CFG}$ discharges until the voltage level, defined by the voltage divider of $R_{1\_CFG}$ and $R_{2\_CFG}$, is reached. The trip level during the on-state of the semiconductor has reached its static level ($V_{CE(ref)}$ = $V_{CE(stat)}$).

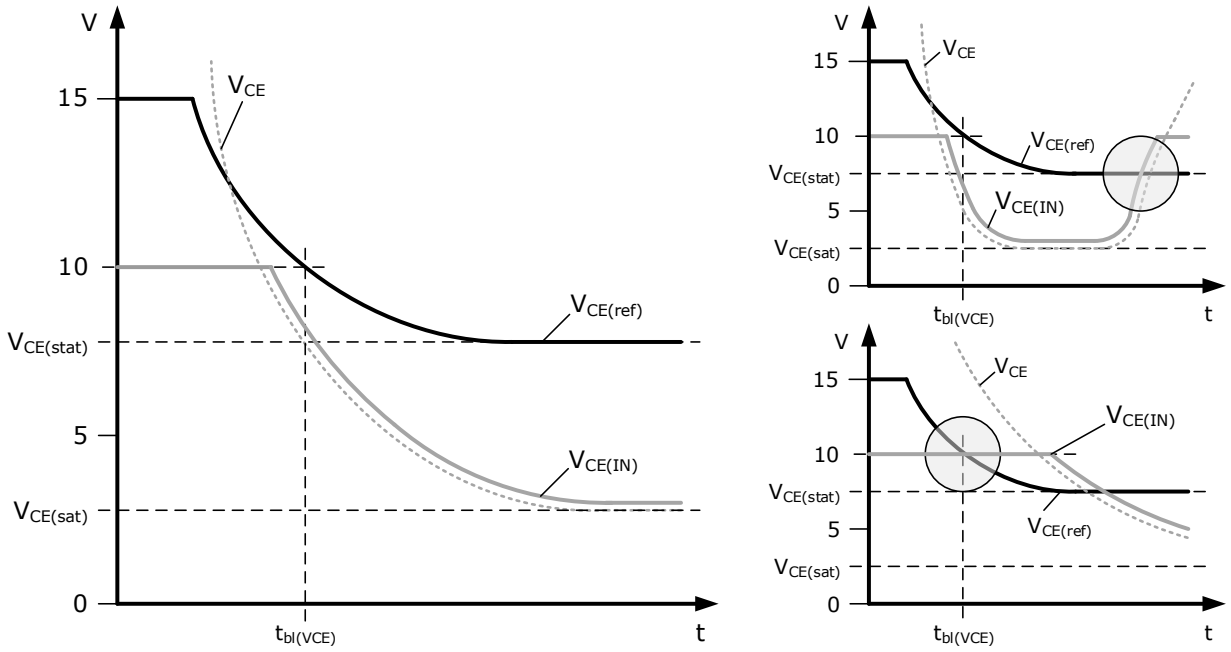
Simultaneously to the discharging process of the capacitor $C_{CFG}$ the semiconductor starts conducting and reducing the collector-emitter voltage $V_{CE}$ to $V_{CEsat}$. When the Collector-Emitter voltage of the IGBT falls below 10V the high-voltage diode $D_{VCE}$ is starting to operate in forward direction. Now, the voltage $V_{CE(IN)}$ at the *VCE_IN* pin follows the collector-emitter voltage of the semiconductor with an offset caused by the forward current $I_F$ of the high-voltage diode $D_{VCE}$ multiplied by the resistance of $R_{VCE}$ plus the voltage drop $V_F$ of the high-voltage diode.

The DSCP feature is active from the moment the voltage $V_{CE(ref)}$ at the *CFG_VCE* pin is below 10V. The time elapsed from initiating the turn-on process of the semiconductor until the DSCP feature is activated is called blanking time $t_{bl(VCE)}$.

In active state the DSCP triggers an error event, if the voltage $V_{CE(IN)}$ at the *VCE_IN* pin exceeds the voltage $V_{CE(ref)}$ of the *CFG_VCE* pin.

Figure 19 shows on the left side the above described process for a well-configured blanking time $t_{bl(VCE)}$ and static threshold voltage $V_{CE(stat)}$.
The upper right side of Figure 19 shows a desaturation event of an IGBT during the DSCP feature is active. In the moment when the voltage $V_{CE(IN)}$ exceeds the threshold voltage $V_{CE(ref)}$ the driver enters into error state.
The lower right side shows an error condition, caused by a too short determined blanking time $t_{bl(VCE)}$. The threshold voltage $V_{CE(ref)}$ has already fallen below 10V before the monitored voltage $V_{CE(IN)}$ is below that level.

**Figure 19: SKYPER® 12 PV | Dynamic short circuit protection**




### 5.5.2 DSCP | Calculation hints

The following equations help to select all relevant parameters of the DSCP feature:

Equation (1) Calculation of the static trip level $(V_{CE(ref)} = V_{CE(stat)})$

$$V_{CE(stat)} = PWR\_VS\_P \cdot \frac{R_{2\_CFG}}{R_{1\_CFG} + R_{2\_CFG}}$$

Equation (2) Calculation of $R_{2\_CFG}$ for a certain value of $V_{CE(stat)}$

$$R_{2\_CFG} = \frac{R_{1\_CFG} \cdot V_{CE(stat)}}{PWR\_VS\_P - V_{CE(stat)}}$$

Equation (3) Calculation of the blanking time $t_{bl(VCE)}$ depending on the values of $C_{CFG}$; $R_{1\_CFG}$; $R_{2\_CFG}$; $V_{CE(stat)}$

$$t_{bl(VCE)} = -C_{CFG} \cdot \frac{R_{1\_CFG} \cdot R_{2\_CFG}}{R_{1\_CFG} + R_{2\_CFG}} \cdot \ln\left(\frac{\frac{10V}{PWR\_VS\_P} \cdot (R_{1\_CFG} + R_{2\_CFG}) - R_{2\_CFG}}{R_{1\_CFG}}\right)$$

Equation (4) Calculation of the voltage $V_{CE(IN)}$ at the *VCE_IN* input depending on the values of $V_{CE}$; $R_{VCE}$; $V_{D\_VCE}$

$$V_{CE(IN)} = \frac{R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}} \cdot V_{CE} + \frac{\left(V_{D\_VCE} + \frac{PWR\_VS\_P \cdot R_{VCE}}{R_1}\right) \cdot R_1 \cdot R_2}{R_1 \cdot R_2 + (R_1 + R_2) \cdot R_{VCE}}$$

## 5.6 Active clamping

The driver offers the possibility to reduce over voltages during the semiconductor's turn-off process by using an active clamping feature. Figure 21 shows an example of an active clamping circuitry based on Zener diodes. The total breakdown voltage of the Zener diodes $D_{CLMP}$ determine the voltage level when the clamping starts. If, during a turn-off of the IGBT the collector-gate voltage $V_{CG}$ raises beyond the break down voltage $V_{Zener}$ the clamping diodes will get conductive. This leads to a current feeding energy into the gate of the IGBT and gradually switches the IGBT on again, until the $V_{CG}$ voltage is reduced below the $V_{Zener}$ reference.
The *CLMP_IN* input indicates the driver that the collector-gate voltage raised above $V_{zener}$, if the voltage at the input exceeds the threshold of 13V. When entering active clamping mode the driver sets the output channels to high impedance, which reduces the losses on the driver.

**Figure 20: SKYPER® 12 PV | Active clamping**

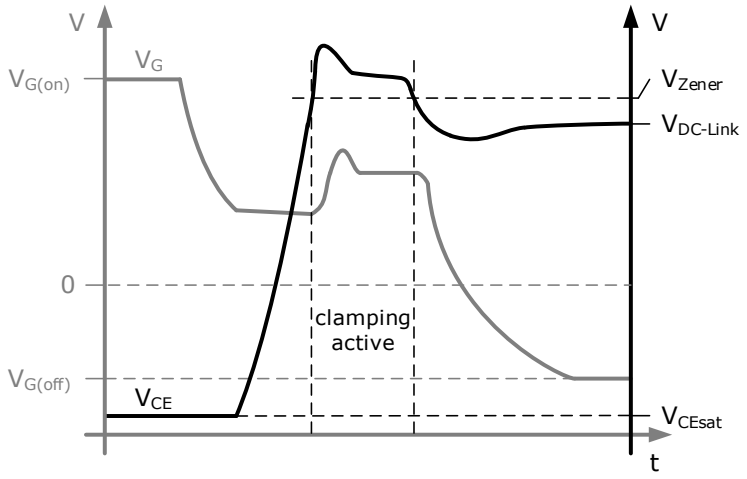
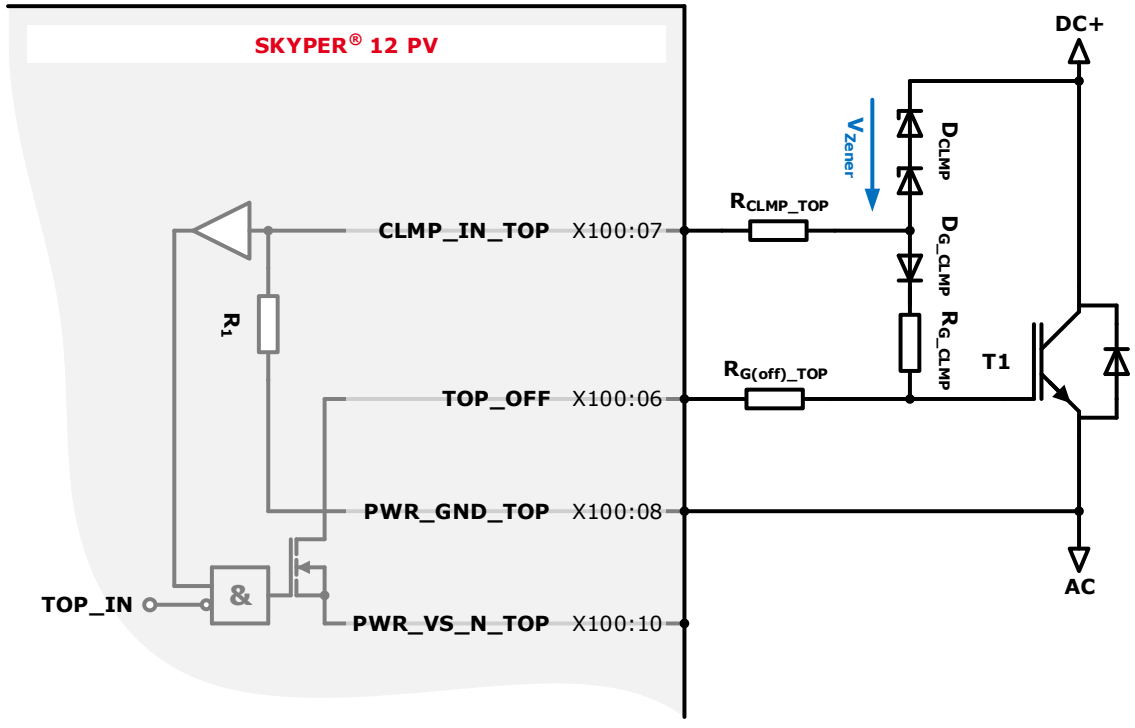



**Figure 21: SKYPER® 12 PV | Application example for active clamping**



**Important Note**
During the clamping process the IGBT is working in a typically not specified linear mode. The suitability of the power semiconductor to operate under such linear conditions, the danger of creating oscillations implying additional considerable loss must be considered and verified. In any case active clamping must not be operated during standard switching to avoid thermal overstress and reduced IGBT lifetime.

| Parameter | Min | Typ | Max |
|---|---|---|---|
| Threshold high CLMP-input | - | - | 13 V |
| Threshold low CLMP-input | 2 V | - | - |

## 5.7 Soft Off

The SKYPER® 12 PV provides a separate turn-off path *TOP_SOFTOFF/BOT_SOFTOFF* activated by the driver, if an error event is detected on the secondary side, as described in chapter 5.1. Switching-off a semiconductor via the soft-off path aims to reduce the switching speed of the semiconductor and, hence, the over voltage caused by the di/dt through the system's stray inductances is decreased.

| Recommendation |
|---|
| Usually the Soft Off resistor is roughly 10 times as high as the standard $R_{G(off)}$. However, the proper value has to be very carefully evaluated in the system in accordance with the individual application parameters. The setup is a balance between staying within the maximum permitted short circuit time of the IGBT and on the other hand reducing the overvoltage below the maximum collector-emitter voltage of the IGBT. Please observe the individual SCSOA of your power semiconductor. |

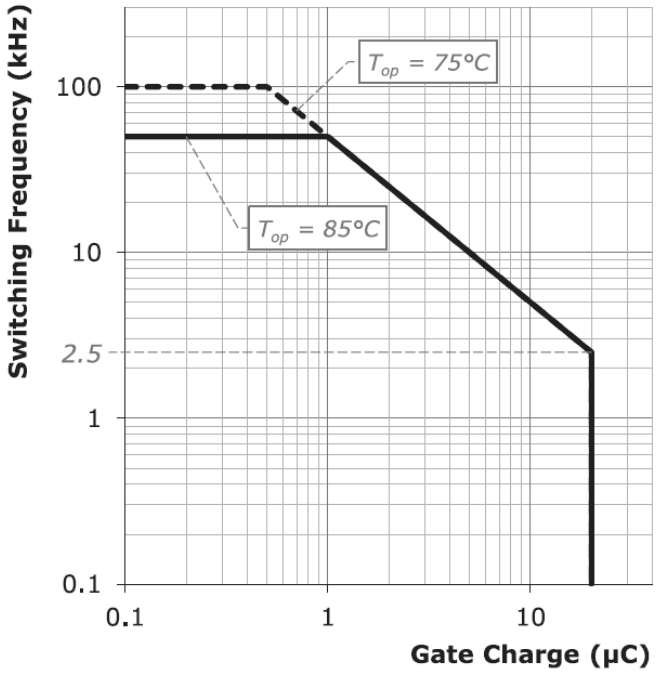
### 5.8 Safe short circuit turn-off in multilevel topology

Power semiconductors in multilevel NPC applications need a careful control, especially in error conditions like a short circuit. A dedicated 3-L topology turn-off sequence avoids damaging the semiconductors due to an unappropriated turn-off sequence. The integrated DSCP, Soft Off and active clamping features ensure that the SKYPER® 12 PV allows proper control of the power semiconductors in multilevel applications. And thanks to the advanced error management provisions realized in the ASIC chipset the SKYPER® 12 PV safely handles even short circuit conditions.

Detailed information how to use the SKYPER® 12 PV driver core in multilevel applications are referred in the Application Note AN19-001 "Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies". Thoroughly reading this document is highly recommended before starting tests of multilevel topologies.

## 6. Electrical characteristic

**Figure 22: SKYPER® 12 PV | Maximum switching frequency**



## 7. Product Qualification

| Table 9: SKYPER® 12 PV \| Routine tests | | | |
|---|---|---|---|
| **test** | **test category** | **test description** | **Standard** |
| AOI | Automated Opt. Inspection | Control of accurate placement of components/ of solder joints, 100% | SEMIKRON |
| ICT | In-Circuit Test | Test of the populated PCB, checking the correctly fabrication, 100% | SEMIKRON |
| FAT | Function Test | Supply current, gate on/off, UVP, error, 100% | SEMIKRON |

| Table 10: SKYPER® 12 PV \| Approval tests | | | |
|---|---|---|---|
| **test** | **test category** | **test description[1]** | **Standard** |
| EP | Electrical Parameters | $\vartheta$amb = -40°C / +85°C | SEMIKRON |
| ST | STEP Test | 20x 10µs to 2s interruption | IEC 61000-4-29 |
| ISO | Isolation | 5.0 kV AC rms, 60s | IEC 62109 |
| TC | Thermal Cycling | 500 cycles a 1h, -40°C – 85°C | IEC 60068-2-14 |
| TH | Temperature Humidity | 85°C, 85% RH, 1000h, passive and at high voltage | IEC 60068-2-67 |
| BST | Burst | Power terminals: 4kV; Control terminals: 2kV | IEC 61000-4-4 |
| CC | Climate Change | -15°C to 85°C; 10% to 85%; 10 cycles a 8h | IEC 60068-2-30 |
| ESD | ESD | Contact discharge: 6kV; Air discharge: 8kV | IEC 61000-4-2 |
| RFF | Radio Frequency | 80 MHz – 1GHz, 20 V/m, 80% AM 1kHz | IEC 61000-4-3 |
| RFD | RF Conducted Disturbance | 150 kHz - 80 MHz, 20 V/m, v+h, 80 % AM 1kHz | IEC 61000-4-6 |
| VB | Vibration | Sinusoidal 20Hz ... 500Hz, 5g<br>26 Sweeps per axis (x, y, z)<br>Random 10Hz … 2000Hz 3g<br>2 h per axis (x, y, z) | IEC 60068-2-6 |
| SH | Shock | Half-sinus pulse, 30g, 6000 shocks, 11ms, ±x, ± y, ± z | IEC 60068-2-27 |

[1] The test conditions are not the maximum applicable conditions for the products. The characteristics of the products are indicated in the data sheet

## 8. Environmental conditions

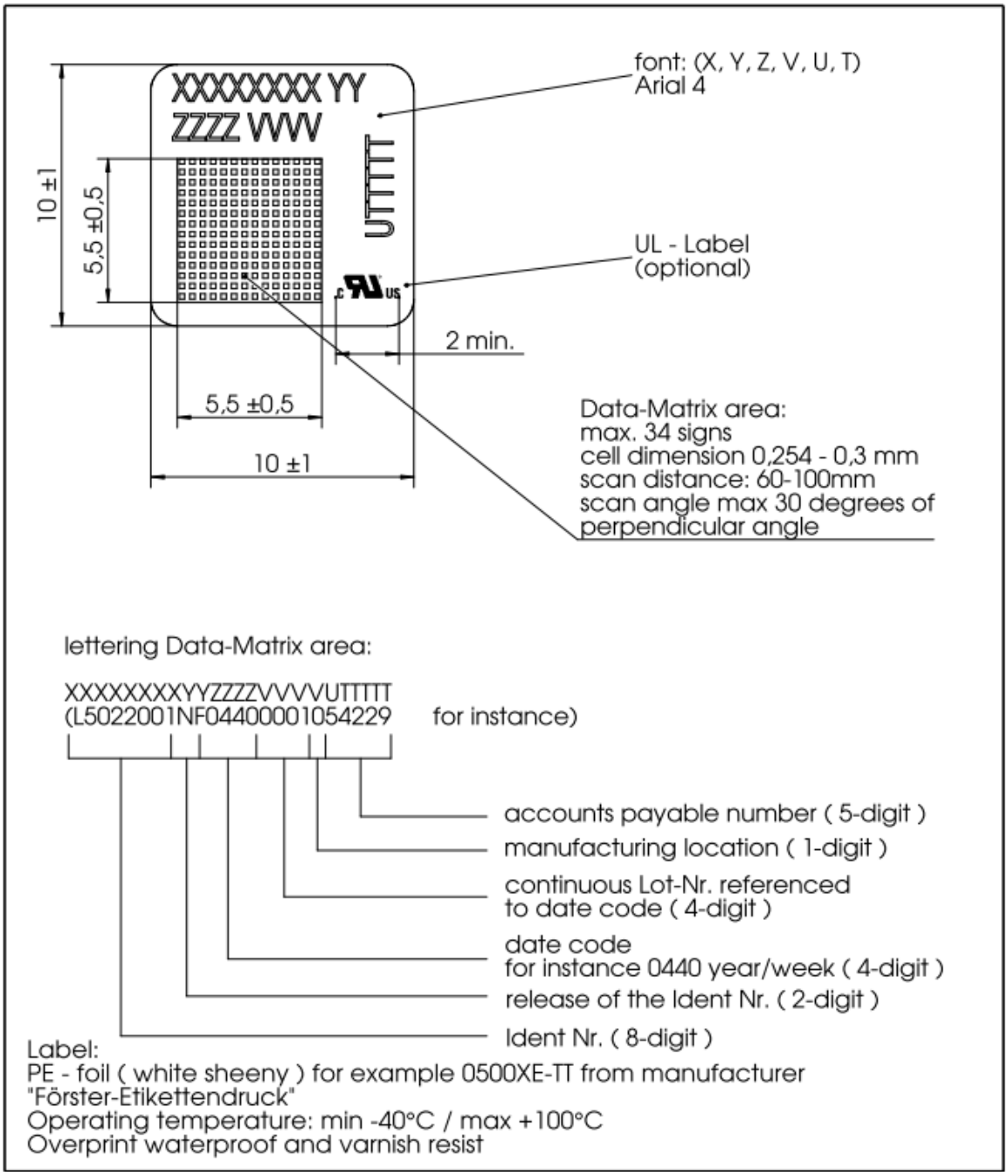
| Table 11: SKYPER® 12 PV \| Environmental conditions | | |
|---|---|---|
| **Insulation parameters** | **Rating** | **Norm / Standard** |
| Grid voltage | 690V | IEC 61800-5-1 |
| Pollution Degree | PD II | IEC 61800-5-1 |
| Maximum altitude | 2000 meter above sea | IEC 61800-5-1 |
| Overvoltage category | OVC III | IEC 61800-5-1 |
| Isolation resistance test, primary to secondary side (2 pieces per lot as series test, power and signal transformers are 100% tested as series test) | 5000 V AC rms, 60s | IEC 61800-5-1 |
| Rated insulation voltage | 8 kV Cat. III | IEC 60664-1 |
| Partial discharge | 2.2kV/1.8kV | IEC 61800-5-1 |
| Creepage distance primary to secondary side | 20.9mm | IEC 61800-5-1 |
| Clearance distance primary to secondary side | 14.0mm | IEC 61800-5-1 |
| Creepage distance secondary to secondary sides | 10.5mm | IEC 61800-5-1 |
| Clearance distance secondary to secondary | 6.1mm | IEC 61800-5-1 |
| CTI rating of the PCB | II (400-600) | IEC 61800-5-1 |
| CTI of the transformers | I (600) | IEC 61800-5-1 |
| **Climate** | **Rating** | **Norm / Standard** |
| Climate class | 3K3 | IEC 60721-3-3 |
| **Environmental conditions** | **Rating** | **Norm / Standard** |
| Operating/storage temperature | -40... +85 °C | |
| High humidity | 85 °C, 85% | |
| Flammability | Heavy flammable materials only | UL94 V0 |
| | | RoHS / WEEE / China RoHS |

| EMC Condition | Rating | Norm / Standard |
|---|---|---|
| ESD | 6 kV contact discharge /<br>8 kV air discharge | IEC 61000-4-2<br>IEC 61800-3 |
| Burst | ≥ 2kV on adaptor board for signals<br>≥ 4kV for AC lines | IEC 61000-4-4<br>IEC 61800-3 |
| Immunity against external interference | ≥ 30V/m<br>80MHz – 1000 MHz | IEC 61000-4-3<br>IEC 61800-3 |
| Immunity against conducted interference | ≥ 20V<br>150kHz – 80MHz | IEC 61000-4-6<br>IEC 61800-3 |
| **Shock Vibration** | **Rating** | **Norm / Standard** |
| Vibration | **Sinusoida**l 20Hz … 500Hz, 5g,<br>26 sweeps per axis (x, y, z)<br>**Random** 10Hz … 2000Hz,<br>3g, 2 h per axis (x, y, z) | IEC 60068-2-6 |
| Shock | 6000 Shocks (6 axis; +-x, +-y, +-z,<br>1000 shocks per axis), 30g, 18ms<br>(The connection between driver and PCB was reinforced by a support post during the test.) | IEC 60068-2-27 |

## 9. Marking

**Figure 23: SKYPER® 12 PV | Label**

Every driver core is marked with a data matrix label. The marking contains the following items.



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[3] P. Bhosale, M. Hermwille, AN-7002 “Connection of Gate Drivers to IGBT and Controller”
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## IMPORTANT INFORMATION AND WARNINGS

The information in this document may not be considered as guarantee or assurance of product characteristics ("Beschaffenheitsgarantie"). This document describes only the usual characteristics of products to be expected in typical applications, which may still vary depending on the specific application. Therefore, products must be tested for the respective application in advance. Application adjustments may be necessary. The user of SEMIKRON products is responsible for the safety of their applications embedding SEMIKRON products and must take adequate safety measures to prevent the applications from causing a physical injury, fire or other problem if any of SEMIKRON products become faulty. The user is responsible to make sure that the application design is compliant with all applicable laws, regulations, norms and standards. Except as otherwise explicitly approved by SEMIKRON in a written document signed by authorized representatives of SEMIKRON, SEMIKRON products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury. No representation or warranty is given and no liability is assumed with respect to the accuracy, completeness and/or use of any information herein, including without limitation, warranties of non-infringement of intellectual property rights of any third party. SEMIKRON does not assume any liability arising out of the applications or use of any product; neither does it convey any license under its patent rights, copyrights, trade secrets or other intellectual property rights, nor the rights of others. SEMIKRON makes no representation or warranty of non-infringement or alleged non-infringement of intellectual property rights of any third party which may arise from applications. This document supersedes and replaces all information previously supplied and may be superseded by updates. SEMIKRON reserves the right to make changes.

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