SEMiSTART® Products

Technical Information

Melanie Gill

December 2009

1 Introduction

SEMiSTART, the anti-parallel uninsulated thyristor module that was designed specifically for use in soft-start devices, boasts one main advantage: compact dimensions. A 400 kW soft-starter featuring SEMiSTART has just one sixth of the volume of the same device with conventional capsule thyristors. Plus, due to pressure contact technology and double-sided chip cooling, these new modules can withstand overload currents of up to 3000 A for a 20 s duration of overload.

1.1 Features

- SEMiSTART modules are available in
  - 3 sizes
  - 5 current classes
  - 2 voltage classes
- Anti-parallel thyristor modules developed for overload conditions
- High load cycle capacity by proven pressure contact technology
- No rating of heat sink necessary due to integrated heat sink
- Low thermal resistance between chip and heatsink beause of double-sided cooling of thyristors
- Thyristors with amplifying gate
- Compact design
- Simple mounting without special tools and thermal paste

1.2 Topology

SEMiSTART products are available as W1C as given below:

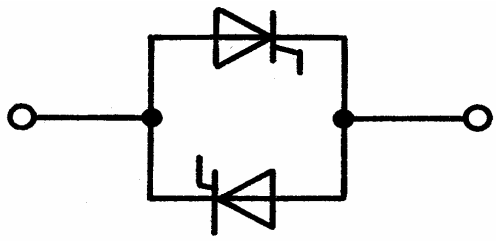


Fig.1-1 SEMiSTART topology

1.3 Type designation

❶	❷	❸	❹	❺
SK	KQ	800	/14	E

❶ SEMIKRON component

❷ W1C, single phase AC controller

❸ $I_{overload}$@W1C, sin 180°, 20s, T_{jmax}=150°C, T_{jstart}=40°C

❹ Voltage class (V_{RRM}[V], divided by 100)

❺ dv/dt class (E: 1000V/µs)

1.4 Typical Applications

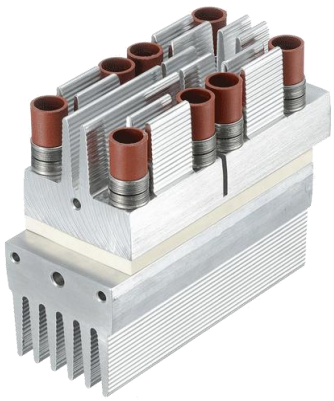
Soft starters for electric motors

2 Mechanical Details

2.1 Dimensions

SEMiSTART has 3 different housing sizes:

SKKQ 560



SKKQ 800/1200/1500

SKKQ 3000

Size	Name	Length (mm)	Width (mm)	Height (mm)
A	SKKQ 560	98	36	100
B	SKKQ 800/1200/1500	123	50	100
C	SKKQ 3000	180	76	160

Fig.2-1 SEMiSTART product family

2.2 Internal construction

In SEMiSTART modules the thyristor chips are directly pressed between two heat sinks using pressure contact technology. The heat sinks also serve as electrical connectors. The modules have few contact layers and no electrical insulation.

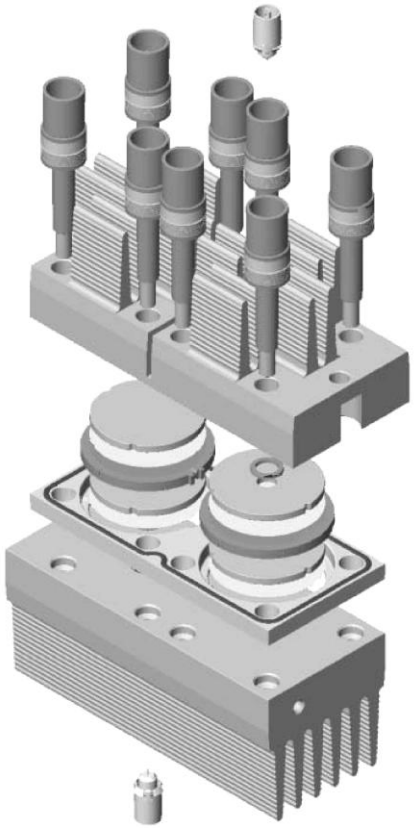


Fig.2-2 SEMiSTART design principle

2.3 Mechanical samples

Following SEMiSTART mechanical samples can be ordered:

Item No.	Name	Size
08282070	SKKQ 560	A
08282080	SKKQ 800/1200/1500	B
08282090	SKKQ 3000	C

Fig.2-3 Item numbers for SEMiSTART mechanical samples

3 Explanation of electrical parameters

3.1 Measuring Thermal Resistance $R_{th(j-s)}$

The definition for thermal resistance R_{th} is the difference between two defined temperatures T divided by the power loss P_V which gives rise to the temperature difference under steady state conditions:

$$R_{th(1-2)} = \frac{\Delta T}{P_V} = \frac{T_1 - T_2}{P_V} \tag{3-1}$$

For SEMiSTART modules the thermal resistance junction to heat sink $R_{th(j-s)}$ is given. The data sheet values base on measured values. As can be seen in equation (3-1), the R_{th} value depends on the temperature difference ΔT, so the reference points have a major influence.

The reference points for SEMiSTART modules are the virtual junction of the chip (T_j) and the lateral surface of the heat sink, where T_s is measured next to the drill hole where the T-sensor is fixed (s. View B in the datasheet). The point for the T_s measurements moves away from the chip with growing modlue size and the thermal resistance rises. For this reason R_{th} can only be used to estimate the chip temperature but not to make a conclusion about the current. This is not necessary because SEMiSTART modules should not be used with continuous load. They absorb heat quite fast and release it again with a time constant that is not of interest for the application.

For further information on the measurement of thermal resistances please refer to:

M. Freyberg, U. Scheuermann, "*Measuring Thermal Resistance of Power Modules* "; PCIM Europe, May 2003

3.2 Transient Thermal Impedance

When switching on a "cold" module, the thermal resistance R_{th} appears smaller than the static value given in the data sheet. This phenomenon occurs due to the internal thermal capacities of the package. These thermal capacities are "uncharged" and will be charged with the heating energy resulting from the losses during operation. In the course of this charging process the R_{th} seems to increase. Therefore it is called transient thermal impedance Z_{th} during the rise time. When all thermal capacities are charged and the heating energy has to be emitted to the ambience, the transient thermal resistance Z_{th} has reached the static data sheet value R_{th}.

This behaviour leads to the advantage of short-term overload capability of the power module.

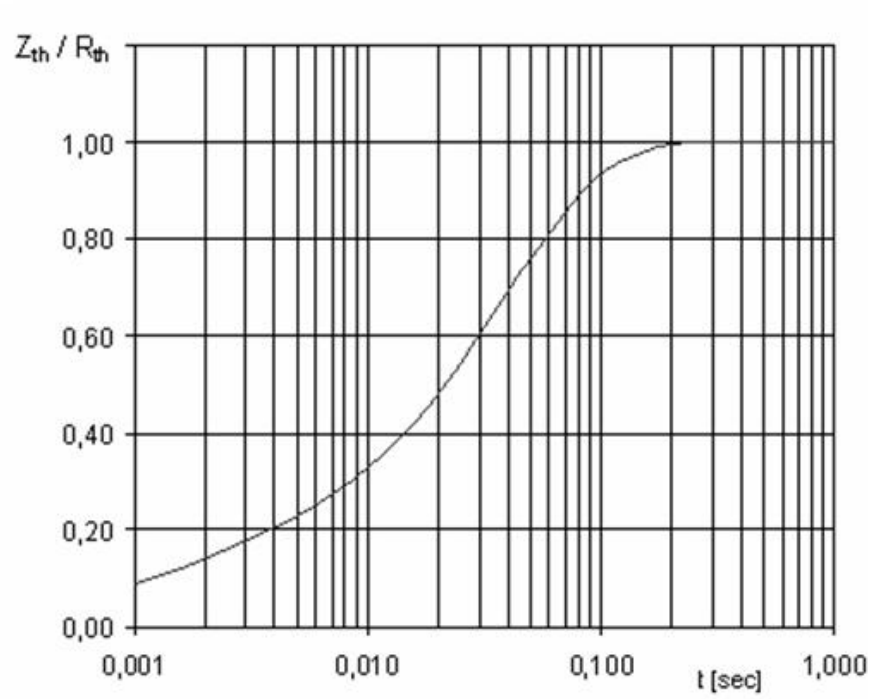


Fig.3-1 Example for the transient thermal impedance

3.3 Explanation of electrical parameters

$I_{overload}$ – overload current

Maximum overload current (rms value). The overload current is limited to 20s only because the junction temperature of the thyristor may rise up to 150°C.

I_{TSM} – surge on-state current

Peak value for a surge current in the form of a single sinusoidal half wave which lasts for 10ms. After occasional current surges with current values up to the given surge forward current, the thyristor can withstand the reverse voltages specified in *Fig. 7* of the datasheets.

i^2t

This value is given to assist in the selection of suitable fuses to provide protection against damage caused by short circuits and is given for junction temperatures of 25°C and 125°C. The i^2t value of the fuse for the intended input voltage and the prospective short circuit in the device must be lower than the i^2t of the thyristor for t = 10ms. When the operating temperature increases, the i^2t value of the fuse falls more rapidly than the i^2t value of the thyristor. A comparison between the i^2t of the thyristor for 25°C and the i^2t value of the (unloaded) fuse is generally sufficient.

V_{RSM} – non-repetitive peak reverse voltage

Maximum permissible value for non-repetitive transient reverse voltages.

V_{RRM} – repetitive peak reverse voltages, V_{DRM} – off-state voltage

Maximum permissible value for repetitive transient off-state and reverse voltages.

T_j – junction temperature

The most important referential value for calculating limiting values is the maximum permissible junction temperature T_j. At a circuit fault (e.g. when a fuse is activated) this value may be exceeded briefly (cf. "surge on-state current").

T_{stg} – storage temperature

The permissible ambient conditions without current or voltage stress are described, among other things, by the maximum permissible storage temperature T_{stg}. The parameter T_{stg} is also the maximum permissible case temperature, which must not be exceeded by an internal or external temperature rise.

V_T – on-state voltage

Maximum forward voltage.

$V_{T(TO)}$ – threshold voltage, r_T – on-state slope resistance

These two values define the forward characteristics (upper value limit) and are used to calculate the instantaneous value of the forward power dissipation P_T or the mean forward power dissipation P_{TAV}:

$$P_T = V_{T(T0)} \cdot I_T + r_T \cdot i_T^2$$

$$P_{TAV} = V_{T(T0)} \cdot I_{TAV} + r_T \cdot I_{TRMS}^2$$

for square-wave pulses: $\frac{I_{TRMS}^2}{I_{TAV}^2} = \frac{360°}{\Theta}$

for [part] sinusoidal half waves: $\frac{I_{TRMS}^2}{I_{TAV}^2} = 2{,}5$ or $\frac{I_{TRMS}^2}{I_{TAV}^2} = \left(\frac{\pi}{2}\right)^2 \cdot \frac{180°}{\Theta}$

Θ: current flow angle

i_T: instantaneous forward current value

I_{TRMS}: RMS on-state current

I_{TAV}: mean on-state current

I_{DD} – direct off-state current

Maximum off-state current for the given temperature and maximum voltage. This value depends exponentially on the temperature.

Time definitions for triggering

Fig. 3-2 shows the characteristics of gate trigger signal V_G and anode-cathode voltage V_{AK} which define the time intervals for the triggering process.

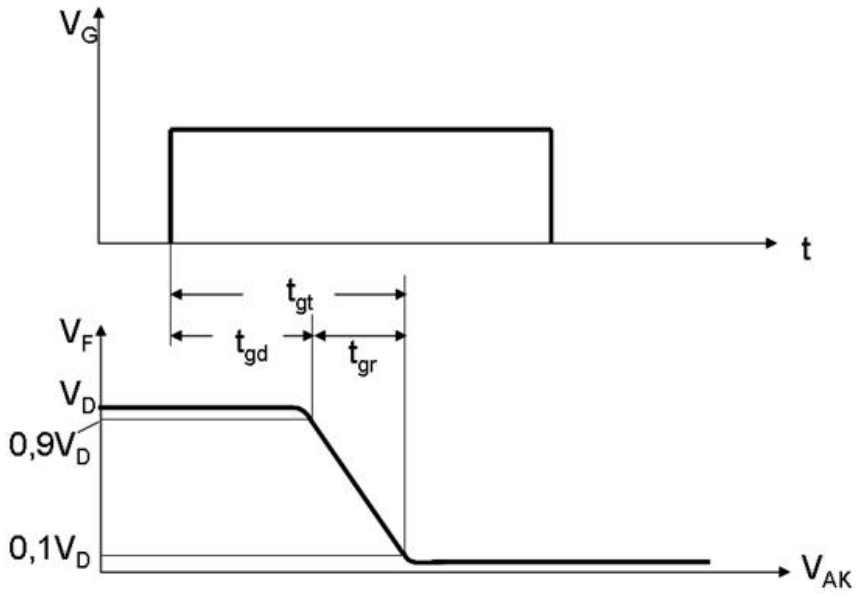


Fig. 3-2 Time definitions for thyristor triggering

t_{gd} – gate-controlled delay time

Time interval between the start of a triggering pulse and the point at which the anode-cathode voltage falls to 90% of its starting value. The datasheet specifies a typical value which is applicable, provided the following conditions are fulfilled:

- Square-wave gate pulse, duration 100µs
- Anode-cathode starting voltage 0.5 V_{DRM}
- On-state current after firing approx. 0.1 I_{TAV} @ 85°C
- Junction temperature during firing approx. 25°C

t_{gr} – gate-controlled rise time

Period within the anode-cathode voltage falls from 90% to 10% of its starting value during firing.

t_{gt} – gate current pulse duration

The sum of the gate controlled delay time t_{gd} and the gate controlled rise time t_{gr}.

$(dv/dt)_{cr}$ – critical rate of rise of off-state voltage

The values specified apply to an exponential increase in off-state voltage to 0.66 V_{DRM}. If these values are exceeded, the thyristor can break over and self trigger.

$(di/dt)_{cr}$ – critical rate of rise of on-state current

Immediately after the thyristor has been triggered, only parts of the thyristor conducts the current flow, meaning that the rate of rise of the on-state current has to be limited. The critical values specified apply to the following conditions:

- repetitive loads with 50-60Hz
- a peak current value corresponding to the crest value of the permissible on-state current for sinusoidal half waves
- a gate trigger current that is five times the peak trigger current with a rate of rise of at least 1A/µs

The critical rate of rise for on-state current falls as the frequency increases, but rises as the peak on-state current decreases. For this reason, for frequencies > 60Hz and pulses with a high rate of rise of current, the peak on-state current must be reduced to values below those given in the datasheets.

t_q – circuit commutated turn-off time

The circuit commutated turn-off time lies in the range of several hundred µs and constitutes the time required for a thyristor to discharge to allow it to take on forward voltage again. This value is defined as the time that elapses between zero crossing of the commutation voltage and the earliest possible load with off-state voltage. In the case of thyristors for phase-commutated converters and a.c. converters, the circuit commutated turn-off time is usually of no significance. For this reason, the datasheets contain typical values only, and no guarantee is given for these values.

I_H – holding current

Minimum anode current which will hold the thyristor in its on-state at a temperature of 25°C. If the thyristor is switched on at temperatures below 25°C, the values specified may be exceeded.

I_L – latching current

Minimum anode current which will hold the thyristor in its on-state at the end of a triggering pulse lasting 10µs. The values specified apply to the triggering conditions stipulated in the section on "Critical rate of rise of on-state current".

V_{GT} – gate trigger voltage, I_{GT} – gate trigger current

Minimum values for square-wave triggering pulses lasting longer than 100µs or for DC with 6V applied to the main terminals. These values will increase if the triggering pulses last for less than 100µs. For 10µs, for instance, the gate trigger current I_{GT} would increase by a factor of between 1.4 and 2. Firing circuits should therefore be arranged in such way that trigger current values are 4 to 5 times larger than I_{GT}. If the

thyristor is loaded with reverse blocking voltage, no trigger voltage may be applied to the gate in order to avoid a non-permissible increase in off-state power losses and the formation of hot spots on the thyristor chip.

V_{GD} – gate non-trigger voltage, I_{GD} – non-trigger current

These trigger voltage and current values will not cause the thyristor to fire within the permissible operating temperature range. Inductive or capacitive interference in the triggering circuits must be kept below these values.

$R_{th(x-y)}$ – thermal resistances, $Z_{th(x-y)}$ – thermal impedances

For SEMiSTART modules thermal resistances/impedances are given for the heat flow between points "x" and "y". Following indices are used:

j - junction

s - sink

a - ambient

The transient thermal impedances $Z_{th(j-s)}$ and $Z_{th(s-a)}$ are shown as a function of time t in *Fig. 3* and *Fig. 4* of the datasheets. For t > 1s, $Z_{th(s-a)}$ of the heat sink must be added to $Z_{th(j-s)}$ in order to calculate the total thermal impedance.

M_t – mounting torque

Tightening torque for terminal screws and fasteners.

m – weight

Weight of the complete module (including heat sink).

Case

Same number means same mechanical features. For details please refer to the drawings in the data sheet.

4 Qualification

4.1 Standard Tests for Qualification

The objectives of the test programme are:

1. To ensure general product quality and reliability.
2. To evaluate design limits by performing stress tests under a variety of test conditions.
3. To ensure the consistency and predictability of the production processes.
4. To appraise process and design changes with regard to their impact on reliability.

Test	Norm	Parameters
High Temperature Reverse Bias	IEC60747	1000h, 66% of voltage class, $105°C \leq T_C \leq 120°C$
High Temperature Storage	IEC60068-2-2	1000h, T_{stgmax}
Low Temperature Storage	IEC60068-2-1	1000h, T_{stgmin}
Thermal Cycling (TC)	IEC 60068-1-14 Test Na	25 cycles, T_{stgmax}-T_{stgmin}
Power Cycling (PC)	IEC60749-34	10000 load cycles, ΔT_j=100K
Vibration	IEC60068-2-6 Test Fc	Sinusoidal sweep, 5g, 2h per axis (x,y,z)
Mechanical Shock	IEC60068-2-27 Test Ea	Half sine pulse, 30g, 3 times each direction (±x, ±y, ±z)

Fig. 4-1 SEMIKRON standard tests for product qualification

SEMiSTART modules have no soft mold protection around the chip. They are therefore susceptible to environmental influences (humidity, dust, etc.). The humidity test according to IEC60068-2-67 is **not** passed by this products.

More details to the above specified quality tests, specific test results and a complete essay for customer presentation are available upon request. Please contact SEMIKRON SEMiSTART Product Management.

4.2 Surge overload current

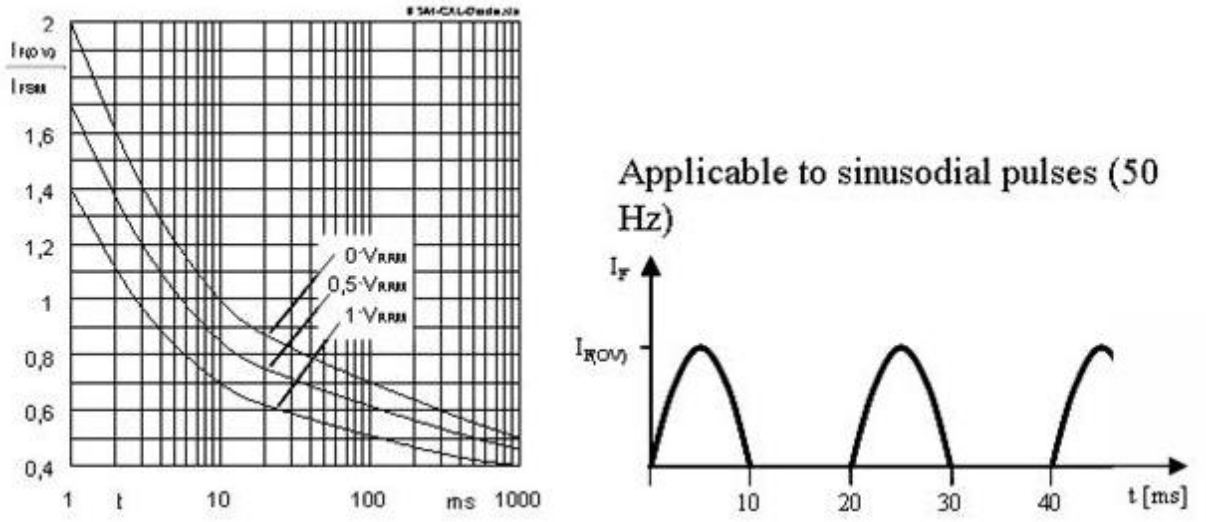


Fig. 4-2 Surge overload current vs. time

Fig. 4-2 shows the peak value of overload current $I_{T(OV)}$ permissible under fault conditions normalised to the surge on-state current I_{TSM} shown as a function of the duration of the fault t. The additional parameter is the peak reverse voltage reapplied immediately after the fault current has ceased. For faults lasting longer than 10ms it is assumed that the current waveform is a series of half sinewaves with a period of 16.6ms respectively 20ms.

Three different curves are shown:

- $0 \cdot V_{RRM}$: no reverse voltage is reapplied
- $½ \cdot V_{RRM}$: a voltage equal to half the repetitive peak reverse voltage rating is reapplied
- $1 \cdot V_{RRM}$: a voltage equal to the full repetitive peak reverse voltage rating is reapplied

4.3 Tests using change of temperature

Since the external contacts have a significantly higher thermal expansion coefficient than the silicon chip, it is apparent that temperature cycling, which stresses these external contacts, is a particularly good test for checking the load cycling stability of the internal contacts. After the testing, the first criteria used for checking whether the contacts have withstood the stresses imposed, is to check the thermal resistance, and additionally the forward and reverse characteristics are checked.

Tests which use external heating and cooling of the component deviate from actual operating conditions in so far as the component under test is uniformly heated and cooled. In reality a varying temperature gradient occurs between the silicon chip and the ambient. Therefore, it is recommended, particularly for a new developed component, to use a further test method, which makes it possible to go through a large number of cycles in a short time with stresses similar to those which occur in the actual working environment. To achieve this, the component under test is brought in close contact with a water cooled

heat sink to keep the case temperature almost constant. By applying short, high current pulses the silicon chip is heated up periodically to almost its maximum allowable virtual junction temperature. During the intervals between the pulses the junction cools down very rapidly. This method produces periodically a high temperature gradient between the silicon chip and the mounting surface.

4.4 Lifetime Calculations

The lifetime of a power module is limited by mechanical fatigue of the package. This fatigue is caused by thermally induced mechanical stress caused by different coefficients of thermal expansion (CTE). In the course of heating (power on) and cooling (power off), the materials expand differently due to their different CTEs. Since the materials are joined, they are unable to expand freely, leading to the mentioned mechanical stress.

The mechanical stresses that occur inside the different material layers, lead to material fatigue when temperature changes. The higher the temperature difference (ΔT), the more stress is induced. With every temperature cycle aging takes place. Wire bonding and solder layers are particularly affected by this. Aging results in small cracks, which start at the edges and extend to the centre of the material with every power cycle that occurs. The higher the medium temperature $T_j m$, the faster the cracks grow, because the activating energy is higher.

The typical defect characteristics resulting from field returns is “lift off” of the wire bonds. This means that the cracks meet in the centre and open the connection in such a way that the wire bond is loose.

This shows that the lifetime is determined by the number of temperature cycles, which can be withstood by the module. In the 1990’s intensive investigations were carried out in this area, including a research project known as the “LESIT study”. One of the main findings of this study was the equation given below (4-1), which shows the relationship between the number of cycles Nf, the junction temperature difference ΔT_j and the medium temperature $T_j m$.

SEMiSTART modules base on the same design principles as the modules, which were investigated in the course of the LESIT study. For this reason the LESIT results may be used for life time estimations. The reliability of power modules has improved since the LESIT study was concluded, so the results of equation (4-1) can be seen as a worst-case scenario.

$$Nf = A \times \Delta T_j^{\alpha} \times \exp\left(\frac{Q}{R \times T_j m}\right) \tag{4-1}$$

A = 640

α = -5

Q = 7.8 10^{-4} J/mol

R = 8.314 J/mol K

ΔT_j and $T_j m$ in [K]

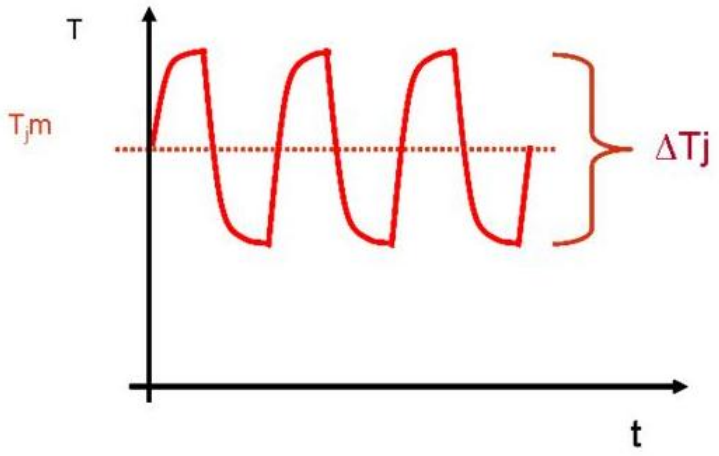


Fig. 4-3 Example of $T_j m$ and ΔT

Fig.4-4 shows the experimental results of the LESIT study (as bullet points) as well as the results of equation 4-1 (as drawn lines).

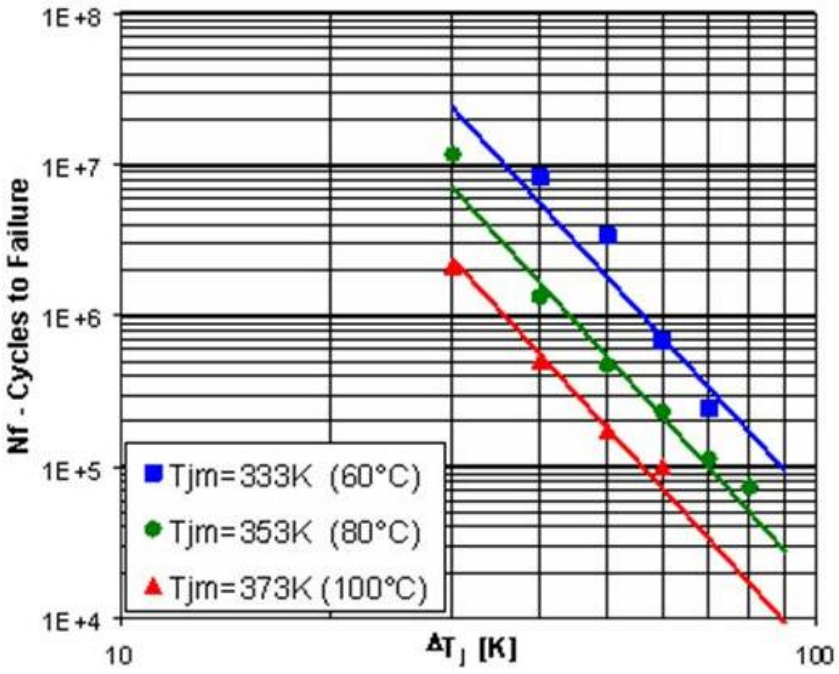


Fig. 4-4 "LESIT" curves, based on experimental results

For further information on the lifetime calculations for power modules please refer to:

M. Held et.al., "*Fast Power Cycling Tests for IGBT Modules in Traction Application*"; Proceedings PEDS, pp 425 – 430, 1997

5 Application

5.1 Overvoltage protection

It is well known that single crystal semiconductor devices are sensitive to over-voltages. Every time their specified reverse voltage is exceeded this can lead to their destruction. It is therefore necessary to protect thyristors against voltage transients however caused, i.e. the transient voltages must be reduced to values below the maximum specified limits for the semiconductor device.

A variety of well tried and tested components is suitable for the above suppression. The most important are:

- resistors and capacitors (RC snubber networks)
- varistors
- silicon avalanche diodes

The RC network operates by forming a series resonant circuit with existing inductances. It transforms any steeply rising transient voltage into a damped sinewave of lower amplitude. The power of the voltage transient is converted from a high value of short duration to a lower value extending over a longer time.

All other components listed above have non-linear characteristics. Their internal resistances reduce when the applied voltage increases. Together with the other resistances and inductances in the circuit, they build non-linear voltage dividers, which allow low voltages to pass unattenuated but clip high voltages above a defined level. The energy of the transient voltage spreads over a longer period again, and is almost completely absorbed by the suppression component.

The suppression components can be positioned on the a.c. side of the thyristor stack, on the d.c. side, or across each semiconductor device in the circuit. The advantages and disadvantages of these various arrangements will be considered separately for each type of suppression component.

RC snubber circuits are often connected in parallel to the thyristor to provide protection from transient overvoltage, although in some cases varistors are used. Due to the RC circuit the rate of rise of voltage is limited during commutation, which reduces the peak voltages across the circuit inductors.

5.2 Over-current and short circuit protection

If short circuit protection is required for the thyristors, (ultra fast) semiconductor fuses are used. These must be dimensioned on the basis of the forward current and i^2t value.

Other types of protection for high current circuits are, for example fuses, which isolate damaged thyristors from the parallel connections. To protect components from statically non-permissible high overcurrents, it is possible to use magnetic or thermal overcurrent circuit breakers of temperature sensors on the heat

sinks, but these do not detect dynamic overload within a circuit. For this reason, temperature sensors are used mainly with forced air cooling in order to protect damage to the thyristors in the event of fan failure.

5.3 Permissible over-currents

The permissible forward currents for short-time or intermediate operation, as well as for frequencies below 40 Hz must be calculated on the basis of the transient thermal impedance or the thermal impedance under pulse conditions so that the junction temperature T_j does not exceed the maximum permissible value at any time.

6 Caption of the figures in the data sheets

Fig. 1 Power dissipation per module vs. rms current

Fig. 2 Power dissipation of three modules vs. rms current

Fig. 3 Transient thermal impedance Zth(j-s) vs. time

Fig. 4 Typical transient thermal impedance Zth(s-a) vs. time (natural cooling)

Fig. 6 Typical overload current vs. time (natural cooling)

Fig. 7 Surge overload current vs. time

Fig. 9 Typical cooling down vs. time (natural cooling)

7 Packaging Information

7.1 **Packaging Unit**

In one box are 3 pieces (valid for all sizes).

Type	**Pieces per box**	**Weight [kg]**
SKKQ 560	3	~1,60
SKKQ 800 / 1200 / 1500	3	~ 3,6
SKKQ 3000	3	~ 10,0

8 Disclaimer

The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliancesand systems is subject to prior specification and written approval by SEMIKRON. Wetherefore strongly recommend prior consultation of our personal.