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# Technical Explanation eMPack A4 Application Kit

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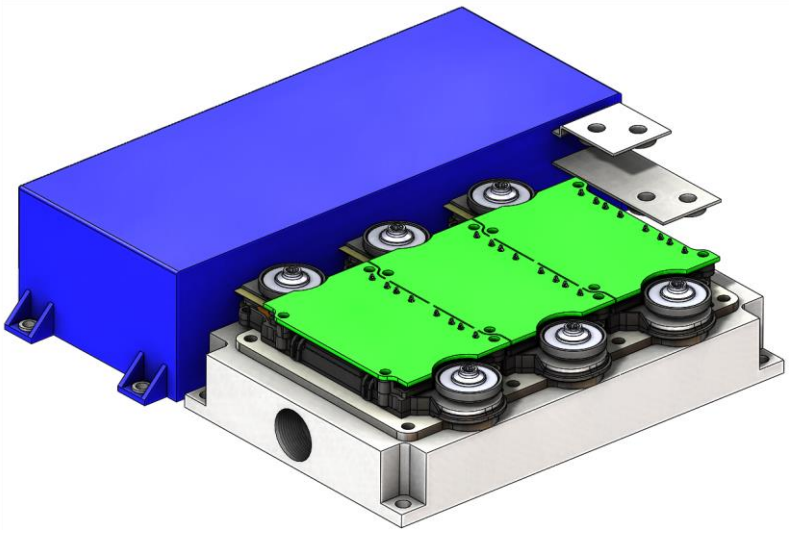
Keyword: eMPack, A4, automotive, IGBT driver, Application Sample

## 1. Introduction

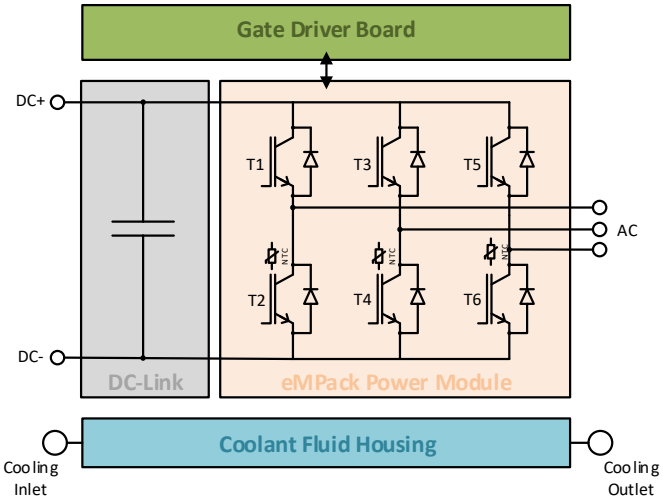
SEMIKRON set up an Application Kit for eMPack modules for evaluation purposes.
The new eMPack module family integrates Semikron's latest DPD (direct pressed die) and DSS (double side sintering) technology in an ultra-low-inductive module design.
While the DPD technology greatly reduces the thermal package resistance, the DSS technology significantly improves the power and temperature cycling capability. The low-inductive module design allows for higher bus voltages and higher output currents resulting in an increased power density. Thus making the eMPack ideal for all kinds of automotive applications.

**Figure 1: Completely assembled eMPack Application Kit**



This Application Sample Kit offers an easy way to set up power inverters with SEMIKRON's eMPack module family.
The Application Kit shall help users to run performance measurements in the lab, build up first demonstration inverters, adjust control algorithms and give some guidance how to build an automotive inverter. However, the kit is not intended for field testing.
All Gate Driver Boards (PCBs only, not mounted to Application Kit) have been isolation tested. There is no functional routine test.

**Figure 2: Application Kit block diagram**



### 1.1 Hardware of the eMPack Application Kit

The Application Kit comprises the following components:

- eMPack Power Module, including mounting screws with isolation sleeves for AC/DC power terminals
- Gate Driver Board
- DC-Link Film Capacitor
- Cooling trough, including gasket and mounting screws

Each of the above mentioned items need to be ordered separately. The order numbers are listed in the following tables.

**Table 1: Order numbers for eMPack power modules and Gate Driver Boards**

| eMPack power module | Description | Order number of power module | Order number of associated Gate Driver Board |
|---|---|---|---|
| eMP1020MD075SC2SV1DPD | SiC, 750V, 1020A | 19285050 | 45152002_01 |
| eMP780MD12SC2SV1DPD | SiC, 1200V, 780A | 19285060 | 45152003_01 |
| eMP1080GD075ED2V1DPD | Si, 750V, 1080A | 19285200 | 45152004_01 |
| t.b.d. | t.b.d. | t.b.d. | t.b.d. |

**Table 2: Order numbers for DC-link capacitors**

| DC-link capacitor | Description | Voltage class | Order number |
|---|---|---|---|
| eMP300-080-APK-DC-CAP | Capacitor 300µF, 800V | Modules with 1200V semiconductors | 19285400 |
| eMP900-045-APK-DC-CAP | Capacitor 900µF, 500V | Modules with 750V semiconductors | 19285401 |

**Table 3: Order numbers for mechanical components**

| Cooling trough | Description | Order number |
|---|---|---|
| eMP-APK-cooling-trough-V1 | Cooling trough for eMPack power modules, gasket, mounting screws | 19285402 |

## 2. Safety Instructions

The eMPack Application Kit bares risks when put in operation. Please carefully read and obey the following safety instructions to avoid harm or damage to persons or gear.
It is in the responsibility of the installer of the eMPack Application Kit to provide a proper design of the test setup. A proper application circuitry shall include safety precautions such as protective fuses and an adequate electrical insulation arrangement.

**Table 4: Safety instructions**

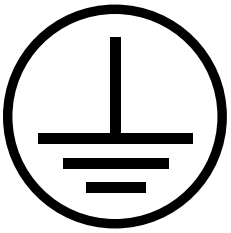
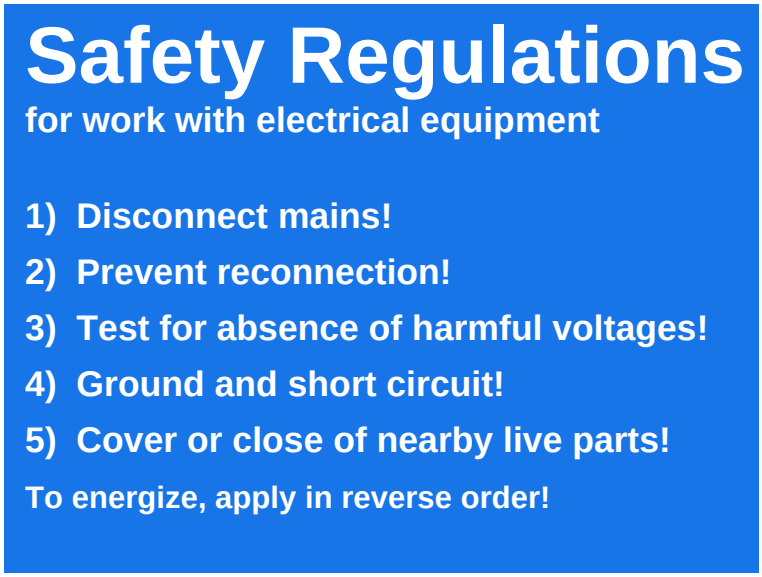
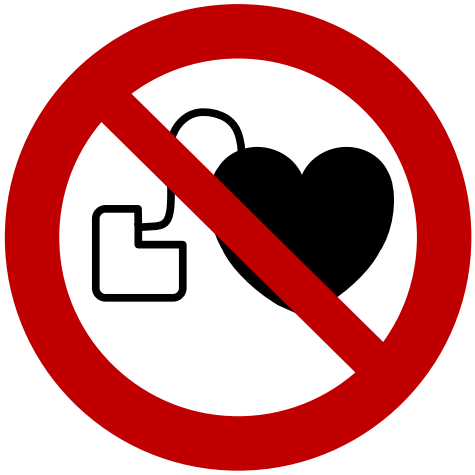
| | |
|---|---|
|  | **In operation the eMPack Application Kit inherits high voltages that are dangerous to life!**<br>**Only qualified personnel should work with the Kit.** |
|  | **Some parts of the eMPack Application Kit or connected devices (e.g. heatsink) may reach high temperatures that might lead to burns when touched.** |
|  | **When connected to DC-link capacitors it must be made sure that the DC-link voltage is reduced to values below 30V before touching the system.** |
|  | **Insulation coordination and testing has been performed regarding a PE connection of one potential. It is mandatory to provide a PE connection with sufficient cross section when operating the eMPack Application Kit.** |

**Table 5: Safety regulations for work with electrical equipment**




Please follow the safety regulations for working safe with the eMPack Application Kit.

**Table 6: No access for people with active implanted cardiac devices!**



Operating the Application Sample may go along with electromagnetic fields which may disturb cardiac devices. People with cardiac devices shall not operate the device.

**Table 7: Handling of ESD sensitive devices**

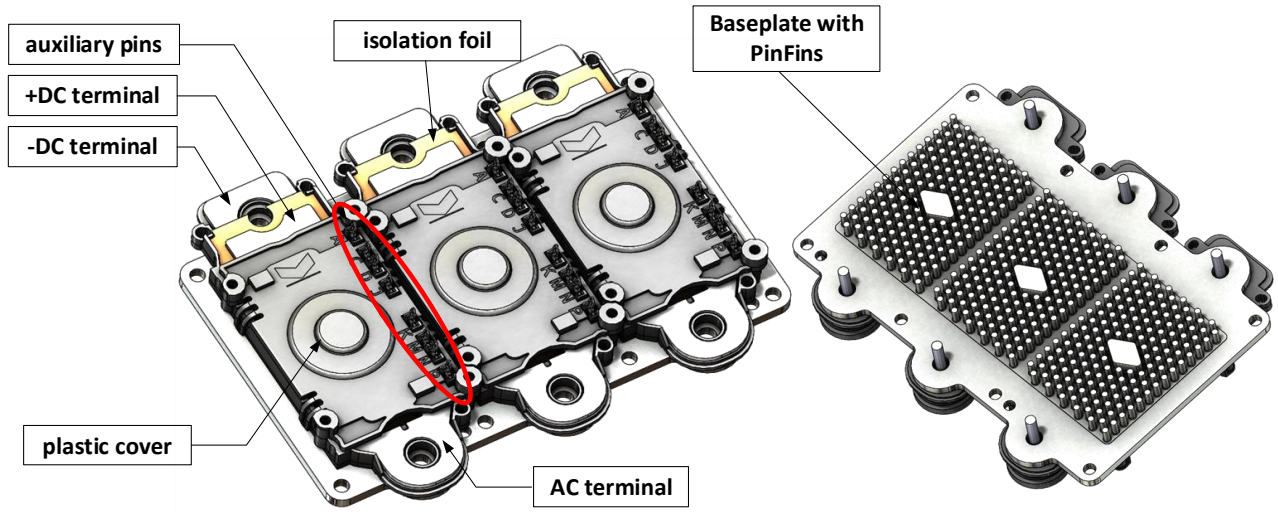
The eMPack power module and Gate Driver Board are sensitive to electrostatic discharge and need to be **ESD protected** during transport and storage!
When handling and assembling the devices it is recommended that a conductive grounded wristlet is worn and a conductive grounded workplace is used. All staff should be trained for correct ESD handling.

# 3. Component Description

## 3.1 eMPack power module

The eMPack module provides overlapping DC-terminals on opposite sides of the AC-terminals. AC- and DC-terminals are fastened by mounting screws with isolation sleeves. The auxiliary contacts are press fit pins. The gate driver board is available as press fit and also as solder version.

**Figure 3: eMPack power module**

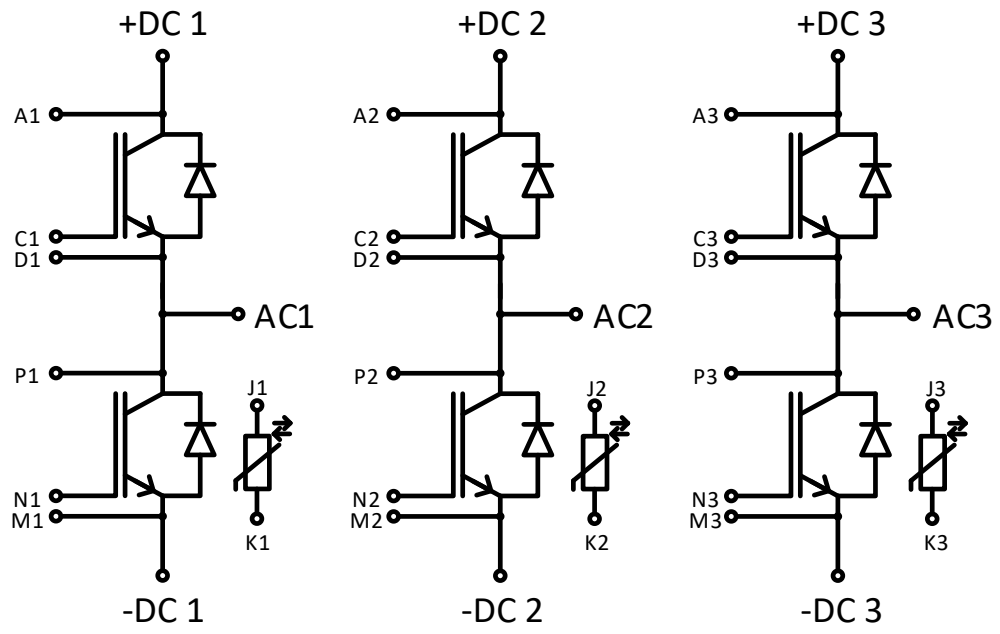



The pinout of the eMPack module is shown in Figure 3 and explained in Table 8.

**Table 8: eMPack pin description**

| Pin | Description Si-version | Description SiC-version |
|---|---|---|
| A | Collector TOP | Drain TOP |
| C | Gate TOP | Gate TOP |
| D | Emitter TOP | Source TOP |
| J | Temp 1 | Temp 1 |
| K | Temp 2 | Temp 2 |
| M | Emitter BOT | Source BOT |
| N | Gate BOT | Gate BOT |
| P | Collector BOT | Drain BOT |
| +DC | DC+ terminals | DC+ terminals |
| -DC | DC- terminals | DC- terminals |
| AC | AC terminals | AC terminals |

**Figure 4: eMPack circuit diagram**



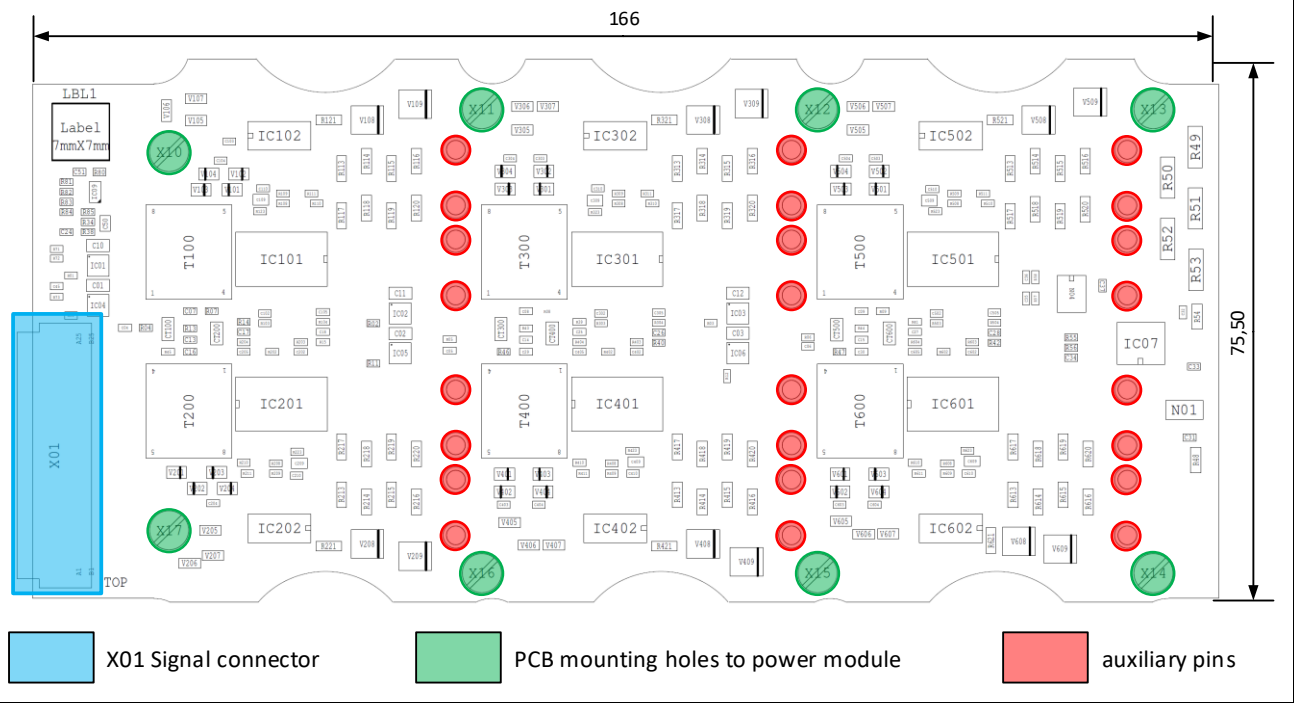

Further information may be found in the module datasheet [1].

### 3.2 Gate Driver Board

The Gate Driver Board comes as an individual component with the eMPack Application Kit. It is 166mm long and 75.5mm wide and perfectly matches the footprint of the eMPack power module.

Figure 5 shows the eMPack Gate Driver Board including the assembly on the TOP side.

**Figure 5: X01-Connector on Gate Driver Board**



The Gate Driver Board has eight 3mm mounting holes (marked in green) for mounting the driver board on the eMPack module during the assembly process.

Detailed information on mounting the Gate Driver Board to the eMPack power module is given in the "eMPack Mounting Instructions" [3].

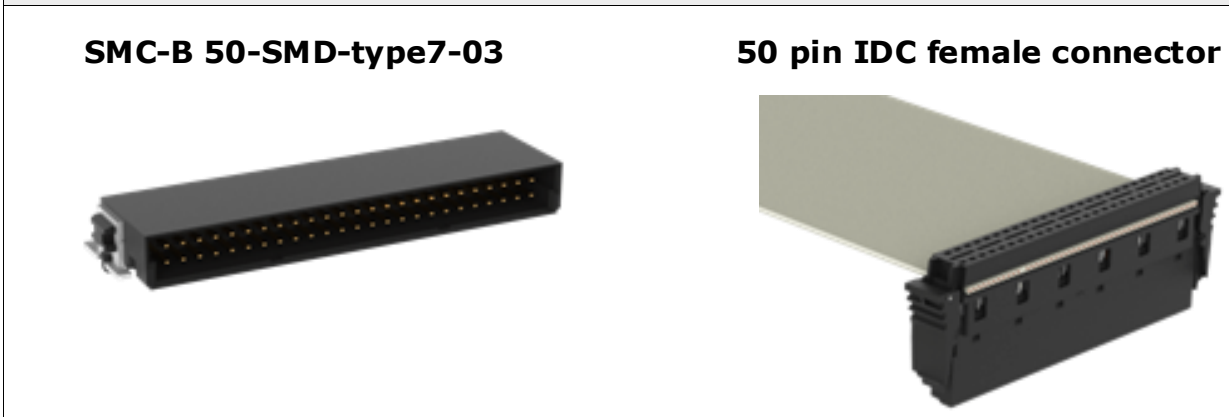
The Gate Driver Board provides a user interface via the 50pin X01 signal connector. Connector type and pin assignment of the X01 connector are described in the following sections.

The functionality of the Gate Driver Board is described in detail in chapter 5.

### 3.2.1 Connector Type

For the X01 connector a 50 pin male SMC-B 50-SMD-type7-03 from ERNI (part number: 154765) is used. Additional information can be found at www.erni.com.

**Figure 6: ERNI male SMC-B 50-SMD-type7-03 (left) and ERNI 50pin IDC female connector (right)**




To connect the X01 connector of the Gate Driver Board a mating 50 pin female counterpart from ERNI shall be used. There are cable assemblies with female connectors in different configurations (standard or crossed) with ribbon cable AWG 30/7 available. For detailed specification and ordering information please refer to the ERNI webpage www.erni.com.

### 3.2.2 Pin assignment

The pin assignment of the X01 signal connector is summarized in the following Table 9.

**Table 9: X01 pin description**

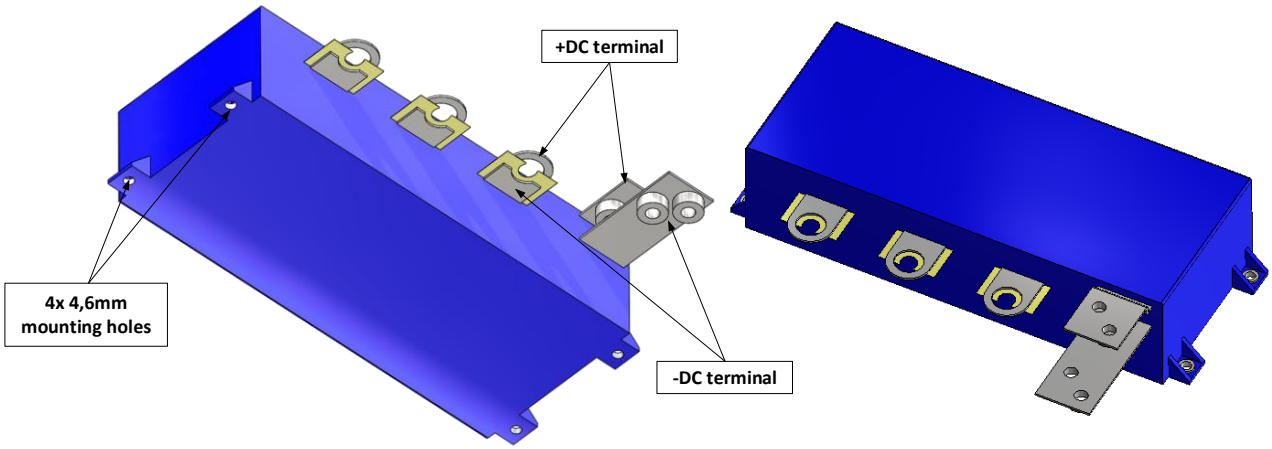
| Pin | Signal name | Description | Direction | Voltage Level |
|---|---|---|---|---|
| A1 | +12V_IN | 12V DC Power Supply | IN | $12V_{DC}$ (-0/+5%) |
| B1 | GND | Ground | - | 0V |
| A2 | +12V_IN | 12V DC Power Supply | IN | $12V_{DC}$ |
| B2 | GND | Ground | - | 0V |
| A3 | +12V_IN | 12V DC Power Supply | IN | $12V_{DC}$ |
| B3 | GND | Ground | - | 0V |
| A4 | +12V_IN | 12V DC Power Supply | IN | $12V_{DC}$ |
| B4 | GND | Ground | - | 0V |
| A5 | +5V | 5V DC Power Supply | IN | $5V_{DC}$ |
| B5 | GND | Ground | - | 0V |
| A6 | NFLTA_LS | Fault A Output of LOW side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | OUT | LOW active, $V_{out,low}$<0.5V |
| B6 | NFLTA_HS | Fault A Output of HIGH side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | OUT | LOW active, $V_{out,low}$<0.5V |
| A7 | NFLTB_LS | Fault B Output of LOW side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | OUT | LOW active, $V_{out,low}$<0.5V |
| B7 | NFLTB_HS | Fault B Output of HIGH side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | OUT | LOW active, $V_{out,low}$<0.5V |
| A8 | NRST_LS_OUT | Reset Input of LOW side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | IN | LOW active, CMOS 5V Level |
| B8 | NRST_HS_OUT | Reset Input of HIGH side switches, Open-Drain, internal $R_{Pullup}$=10kΩ | IN | LOW active, CMOS 5V Level |
| A9 | EN | Enable Input Disable=0V / Enable=5V | IN | CMOS 5V Level |
| B9 | NFLT_PSU | Fault signal of PSU transformer driver Open-Drain | OUT | LOW active, TTL 5V Level |
| A10 | GND | Ground | - | 0V |
| B10 | GND | Ground | - | 0V |
| A11 | PWM_TOP1 | PWM Signal TOP switch Phase U Off=0V / On=5V | IN | CMOS 5V Level |
| B11 | PWM_BOT1 | PWM Signal BOT switch Phase U Off=0V / On=5V | IN | CMOS 5V Level |

| Pin | Signal name | Description | Direction | Voltage Level |
|---|---|---|---|---|
| A12 | PWM_TOP2 | PWM Signal TOP switch Phase V<br>Off=0V / On=5V | IN | CMOS 5V Level |
| B12 | PWM_BOT2 | PWM Signal BOT switch Phase V<br>Off=0V / On=5V | IN | CMOS 5V Level |
| A13 | PWM_TOP3 | PWM Signal TOP switch Phase W<br>Off=0V / On=5V | IN | CMOS 5V Level |
| B13 | PWM_BOT3 | PWM Signal BOT switch Phase W<br>Off=0V / On=5V | IN | CMOS 5V Level |
| A14 | GND | Ground | - | 0V |
| B14 | GND | Ground | - | 0V |
| A15 | CLK_IN | SPI Serial Clock | IN | CMOS 5V Level |
| B15 | GND | Ground | - | 0V |
| A16 | NCS_IN | SPI Chip Select | IN | CMOS 5V Level |
| B16 | GND | Ground | - | 0V |
| A17 | SDI | SPI Serial Data Input | IN | CMOS 5V Level |
| B17 | GND | Ground | - | 0V |
| A18 | SDO | SPI Serial Data Output | OUT | CMOS 5V Level |
| B18 | GND | Ground | - | 0V |
| A19 | RESERVED | RESERVED | - | - |
| B19 | RESERVED | RESERVED | - | - |
| A20 | RESERVED | RESERVED | - | - |
| B20 | RESERVED | RESERVED | - | - |
| A21 | NEN_PSU_IN | Enable Input for PSU Transformer Driver | IN | LOW active,<br>TTL 5V Level |
| B21 | V_DC_LINK1 | DC-Link voltage measurement 1 | OUT | 0..5V analogue output |
| A22 | V_DC_LINK2 | DC-Link voltage measurement 2 | OUT | 0..5V analogue output |
| B22 | RESERVED | RESERVED | - | - |
| A23 | TEMP_PH_U1 | DCB-Temperature Phase U pos. | OUT | 4.7kΩ ± 1% @ $T_r$=25°C |
| B23 | TEMP_PH_U2 | DCB-Temperature Phase U neg. | OUT | |
| A24 | TEMP_PH_V1 | DCB-Temperature Phase V pos. | OUT | 4.7kΩ ± 1% @ $T_r$=25°C |
| B24 | TEMP_PH_V2 | DCB-Temperature Phase V neg. | OUT | |
| A25 | TEMP_PH_W1 | DCB-Temperature Phase W pos. | OUT | 4.7kΩ ± 1% @ $T_r$=25°C |
| B25 | TEMP_PH_W2 | DCB-Temperature Phase W neg. | OUT | |

### 3.2.3 DC-Link film capacitor

The eMPack DC-link capacitor is shown in Figure 7. Due to the overlapping DC terminals the eMPack DC-link capacitor provides a very low leakage inductance, perfectly matched to the low-inductive module terminal layout.

**Figure 7: DC-link capacitor interface**




The +/-DC terminals on the user side each provide two M5 press nuts for connecting the HV battery or HV power supply. The capacitor also provides four 4.6mm mounting holes allowing the user to mount it to a heat sink.

The DC-Link capacitor is available in two versions (depending on the power module voltage class):

**Table 10: DC-link film capacitor specification**

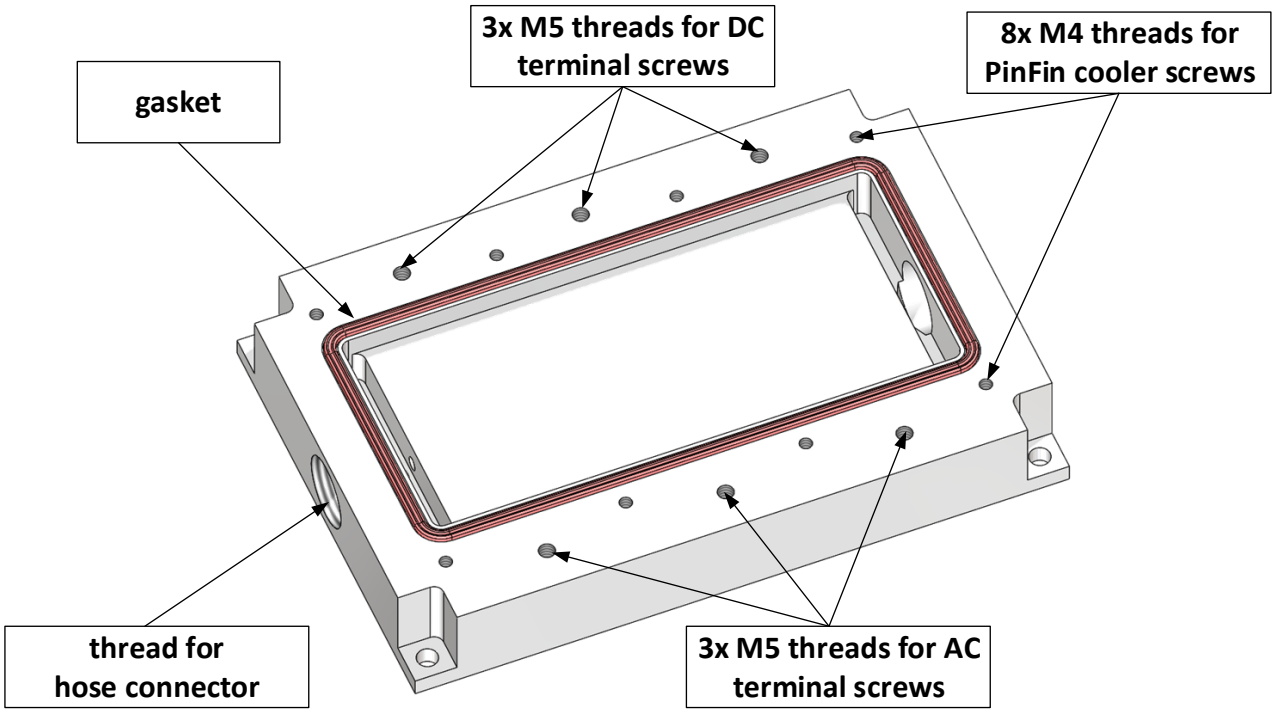
| | **eMP300-080-APK-DC-CAP** | **eMP900-045-APK-DC-CAP** |
|---|---|---|
| **nom. DC-Link voltage** ($V_r$) | 500V | 750V |
| **max. DC-Link Voltage** ($V_{max}$) | 600V | 900V |
| **Capacitance** ($C_r$) | 900µF | 300µF |

Further information such as mechanical dimensions can be found in the "eMPack mounting Instructions" [3].

## 3.3 Coolant fluid housing

The coolant fluid housing of the eMPack Application Kit comprises a relief matched to the PinFin area of the eMPack baseplate. A gasket around the relief seals the connection between coolant fluid housing and coolant plate. The housing provides 8x M4 threads for the coolant plate, 6x M5 threads for the AC/DC terminal screws and two ½ inch sized screw threads for the hose connectors. The coolant fluid housing is shown in Figure 8.

**Figure 8: Cooling trough**




The coolant circuit of the eMPack Application Kit contains the following parts:

**Table 11: Cooling trough**

| Cooling trough | Description | Order number |
|---|---|---|
| eMP-APK-cooling-trough-V1 | Cooling trough for eMPack power modules, gasket, 8x M4 mounting screws | 19285402 |

Regarding the selection of the coolant type the used materials of the cooling circuit need to be considered. The user has to ensure that the used coolant medium is compatible with the cooling circuit materials to avoid e.g. corrosion or freezing at low temperatures. SEMIKRON proposes the usage of a mixture of water and glycol with corrosion inhibitor. Percentage of glycol should be at least 10%.

For ongoing information and hints concerning cooling circuit / coolant please refer to SEMIKRON Application manual for Power Semiconductors [2].
Further information such as mechanical dimensions can be found in the "eMPack Mounting Instructions" [3].

## 4. Assembly

Before setting up the electrical connection, the Application Kit must be assembled as described in the document "eMPack Mounting Instructions" [3].
All components need to be installed. **It is in the user's responsibility to provide a proper and save design of the test setup.**
Please carefully read and obey the safety instructions in chapter 2 of this document to avoid harm or damage to persons or gear.

### 4.1 Isolation test

**After assembling the eMPack Application Kit the user must perform an isolation test of the complete kit to eliminate errors during the mounting process and ensure safe operation.**
One electric pole of the test voltage of 1500$V_{AC}$ must be connected to the 50-pin primary plug X01 shorting all 50 pins (low voltage / primary side). The other electric pole contacts all high voltage (secondary side) terminals (all +DC, all –DC, all AC terminals and the heat sink). The test voltage must be applied to the device-under-test for 6s and the leakage current may not exceed 3mA.
**If the leakage current exceeds this limit the Application Kit very likely has an isolation fault. Please do not apply high voltage!**

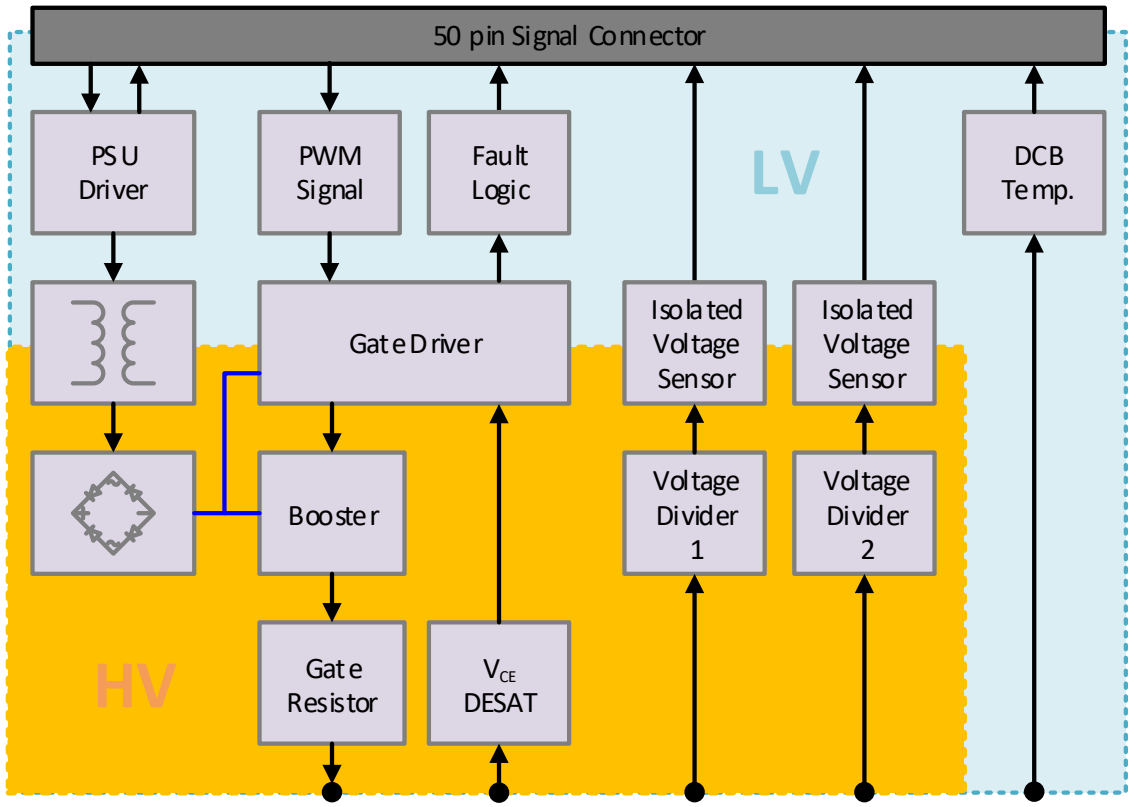
## 5. Gate Driver Functionality

### 5.1 Driver block diagram

Due to the very compact design of the new eMPack module family the available space for the Gate Driver Board is limited respectively. The Gate Driver Board of this eMPack Application Kit shall prove the feasibility of covering relevant functional safety requirements according to automotive standards (as per ISO26262) on a limited PCB footprint resulting in a very compact overall system design.

The Gate Driver block diagram in Figure 9 shows high voltage side (primary side, HV) and low voltage side (primary side, LV). Both HV and LV section are galvanically insulated as described in section 6.3.

**Figure 9: Gate Driver block diagram**



## 5.2 Power supply

### 5.2.1 Primary side power supply

The gate driver primary side is powered by the 5V supply voltage on the X01 connector. It mainly consists of the isolated gate drivers (1EDI2002AS) and isolated voltage sensors (ACPL-C87B).
A regulated 5V supply voltage needs to be applied by the user on the respective pins on the X01 connector. For detailed pin description please refer to Table 9.

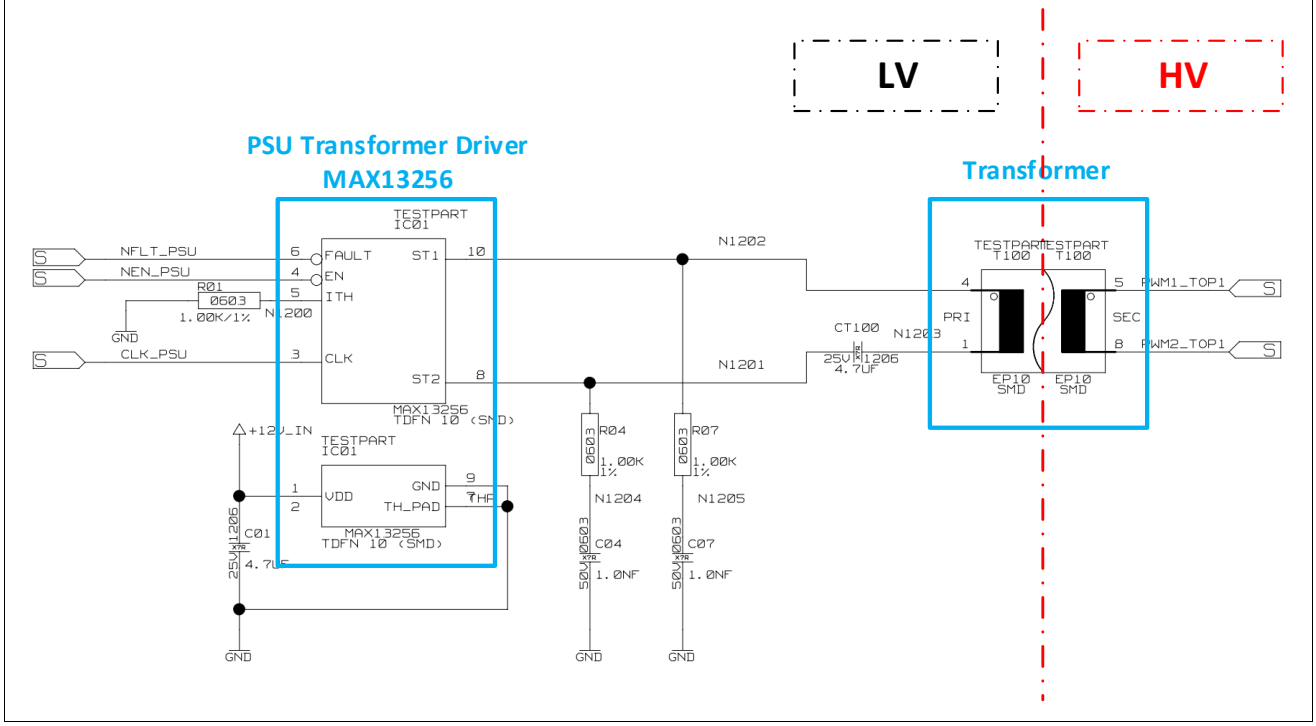
### 5.2.2 Secondary side power supply

The gate driver secondary side power supply is built up with the PSU transformer driver MAX13256 from Maxim Integrated. Each of the six module switches comprises a PSU transformer driver with an individual transformer. The MAX13256 provides the following signals for control and feedback purposes on the X01 connector:

| Signal | Function | Description |
|---|---|---|
| NFLT_PSU | LOW active Fault Output | The fault signal turns low when there is either an over temperature or overcurrent condition detected by one of the six PSU Transformer Drivers |
| NEN_PSU_IN | LOW active Enable Input | A LOW signal needs to be applied in order to enable all six Transformer Drivers. Applying a HIGH signal (5V) will disable the devices. |

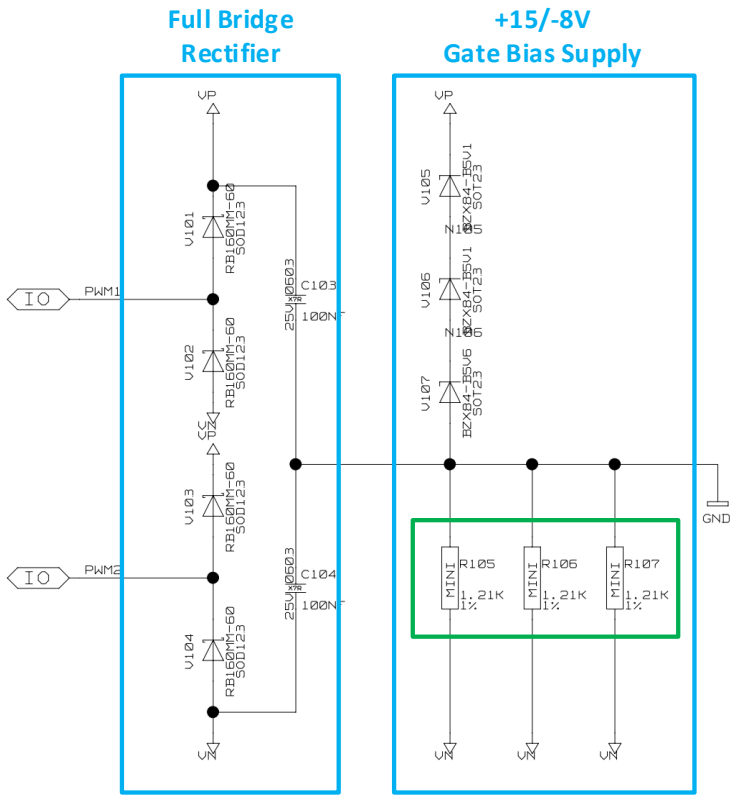
The MAX13256 is supplied by the 12V supply voltage on the X01 connector. The 12V supply voltage should be applied to the X01 connector prior to enabling the PSU via the NEN_PSU_IN signal. Figure 10 shows an excerpt of the PSU schematics.

**Figure 10: Secondary side power supply schematics**




On the gate driver secondary side a full bridge rectifier is used. The gate bias supply voltage is generated by a series connection of three Zener diodes with three paralleled resistors (framed in green in Figure 11). The three resistors at the switches T1–T5 are 3x 1.21kΩ. Due to the additional load for the DC-Link voltage measurement the three resistors at switch T6 are 3x 560Ω.

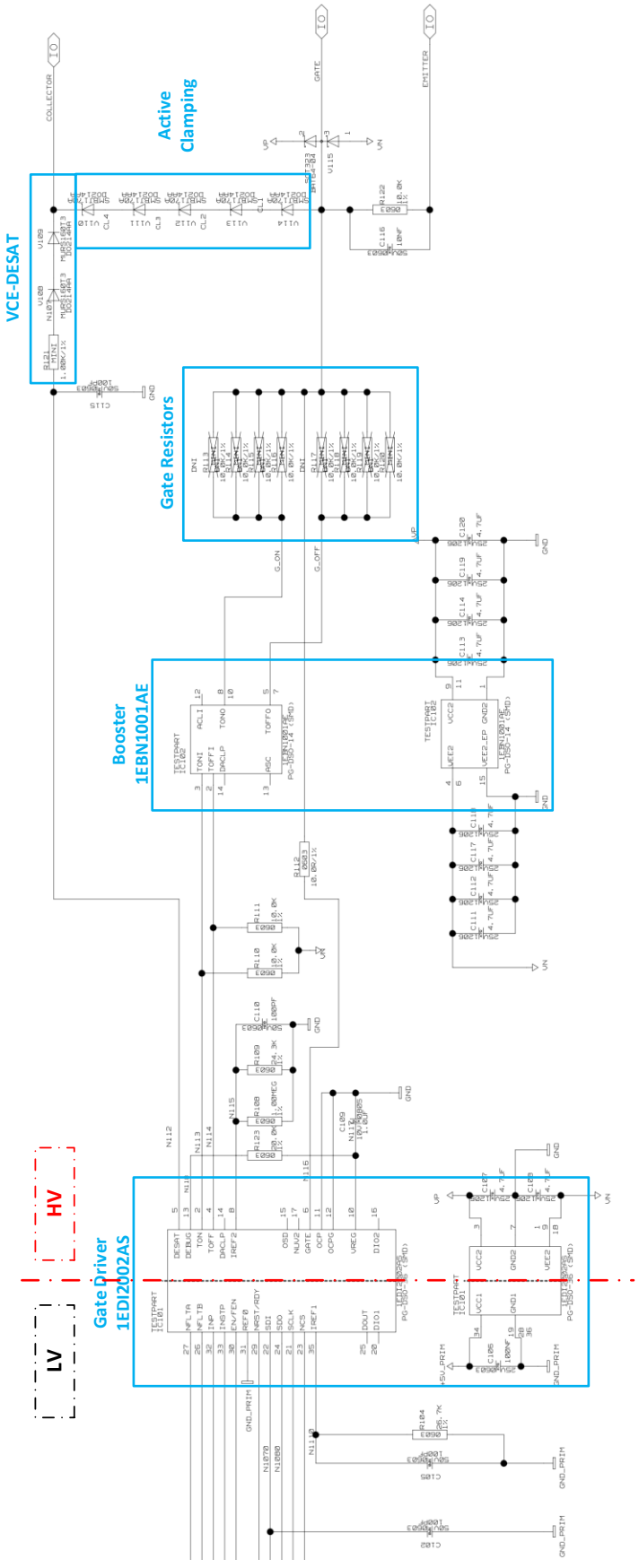
**Figure 11: Secondary side rectifier and gate bias supply**




## 5.3 Gate Driver stage

The Gate Driver stage is built on the Infineon EiceDRIVER 1EDI2002AS and an external bipolar booster 1EBN1001AE. The 1EDI2002AS is a high-voltage IGBT gate driver designed for automotive motor drives. It implements a panel of safety-related functions in order to support functional safety requirements at system level (as per ISO 26262). The 1EBN1001AE is also designed for automotive motor drives applications and is able to drive and sink currents up to 15A. The 1EBN1001AE supports additional features (which are not realized in this design) in order to make it suitable for safety related system designs.

**Figure 12: Gate driver schematics**



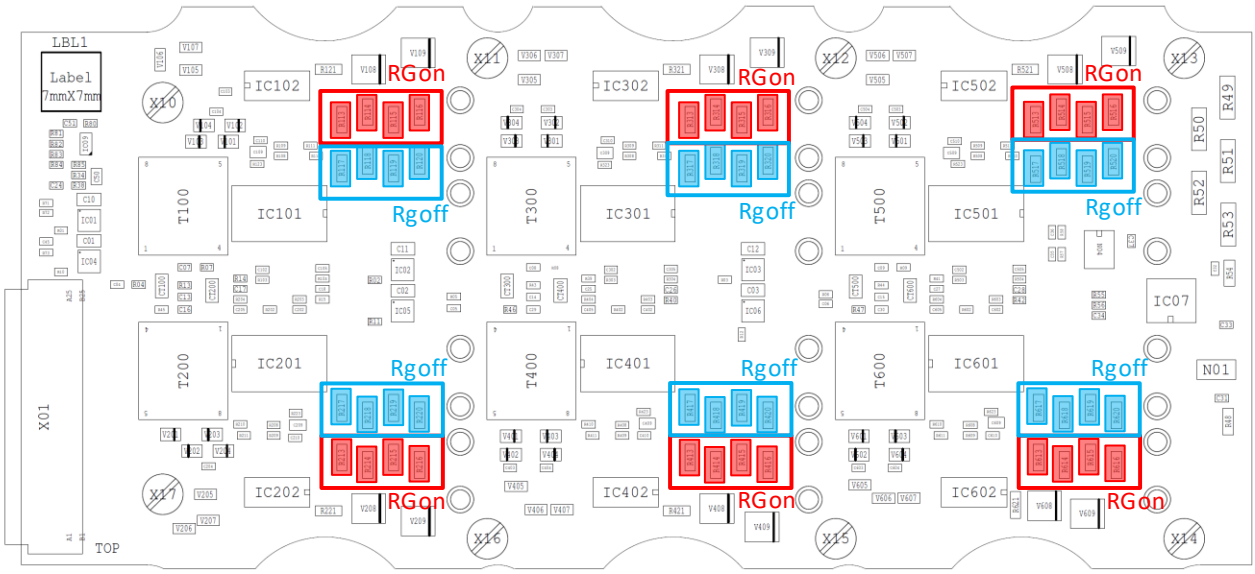
### 5.3.1 Gate resistors

Several chips on the Driver Board realize what is called gate resistor in this document for the sake of convenience. The Driver Board offers separate placement positions for turn-on ($R_{G,on}$) and turn-off ($R_{G,off}$) resistors. The $R_{G,on}$ resistor is used for every turn-on process, $R_{G,off}$ for every turn-off action.

**Turn-on resistor ($R_{G,on}$)**
The driver board offers four pads per IGBT for the turn-on resistor $R_{G,on}$ (framed red in Figure 13) taking MiniMELF (0204) components. Resistor values need to be chosen according to the particular application (DC-link voltage, switching frequency, switching losses, etc.). SEMIKRON has already evaluated suitable resistance values for different power modules. Please refer to Table 12 for factory settings.

**Turn-off resistor ($R_{G,off}$)**
The driver board offers four pads per IGBT for the turn-off resistor $R_{G,off}$ (framed blue in Figure 13) taking MiniMELF (0204) components. Resistor values need to be chosen according to the particular application (DC-link voltage, switching frequency, switching losses, etc.). SEMIKRON has already evaluated suitable resistance values for different power modules. Please refer to Table 12 for factory settings.

**Figure 13: Gate resistor placement position on PCB top side**




For proper operation all placement positions must be populated. Factory settings for the turn-on and turn-off resistors are summarized in the following Table 12:

**Table 12: Gate resistor factory settings**

| Module Type | Voltage Class | Resistor Package | $R_{G,on}$ | $R_{G,off}$ |
|---|---|---|---|---|
| eMP1020MD075SC2SV1DPD | 750V | 4x0204 (Mini MELF) | t.b.d. | t.b.d. |
| eMP780MD12SC2SV1DPD | 1200V | 4x0204 (Mini MELF) | t.b.d. | t.b.d. |
| eMP1080GD075ED2DPD | 750V | 4x0204 (Mini MELF) | t.b.d. | t.b.d. |
| t.b.d. | t.b.d. | t.b.d. | t.b.d. | t.b.d. |

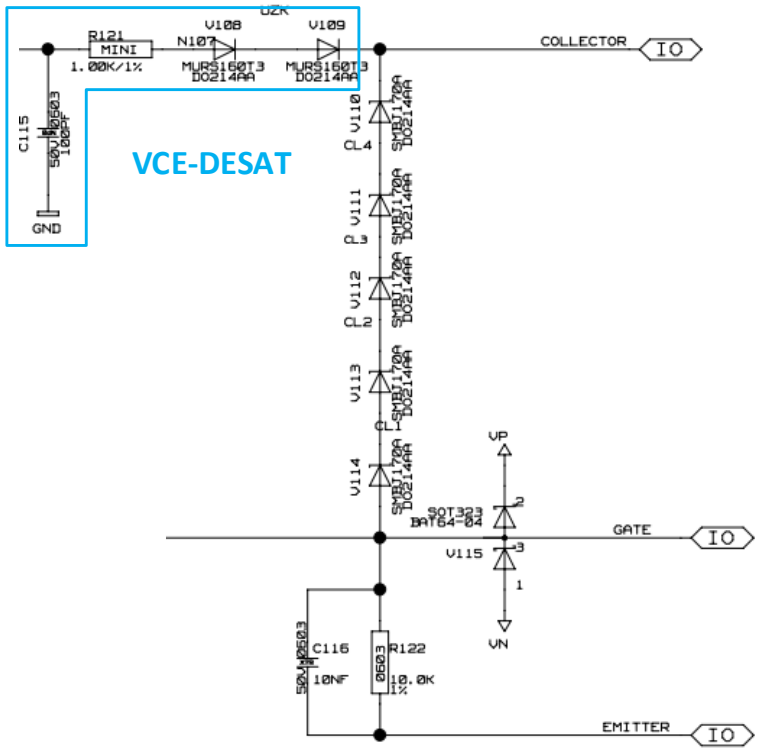
**Safe turn-off feature**
In case of an error a Gate Driver typically uses a so called soft-off resistor instead of the above mentioned $R_{G,off}$ in order to switch off the device smoothly and avoid any critical over voltages.
This Driver Design does NOT use any soft-off resistors. For critical events the Infineon Gate Driver offers a so called safe turn-off sequence which switches off the device with the Two Level Turn-Off functionality.

**This feature is deactivated by default and needs to be configured and activated via SPI interface first.**
**For details please refer to the Infineon 1EDI2002AS datasheet [4].**

### 5.3.2 $V_{CE}$-DESAT protection

The DESAT function implemented in the 1EDI2002AS Gate Driver aims at protecting the IGBT in case of a short circuit. The $V_{CE}$ voltage drop over the IGBT is monitored via the DESAT pin while the device issues a PWM ON command. The voltage at pin DESAT is filtered by an external RC filter (1kΩ/100nF), and decoupled by a series connection of two external diodes (MURS160T3). Figure 14 shows an excerpt of the schematics.

**Figure 14: VCE DESAT schematics**



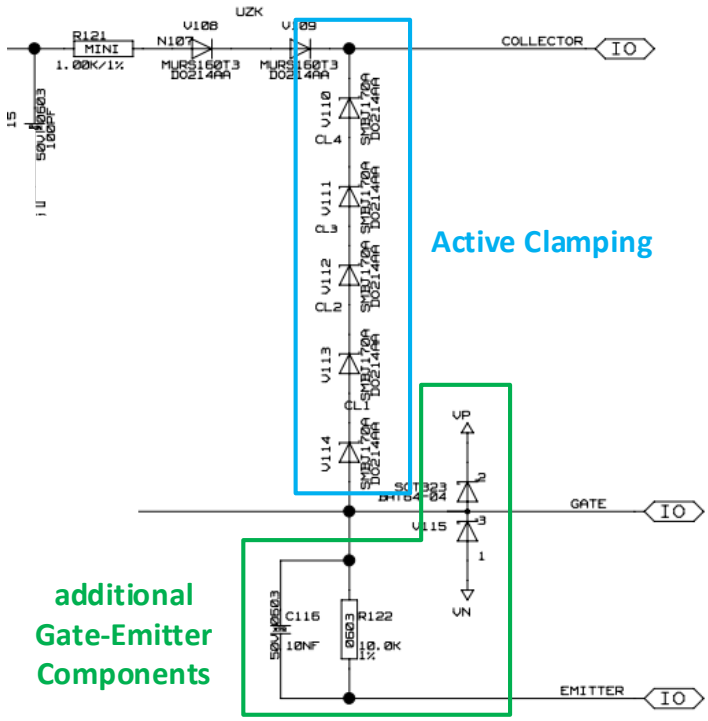

At the beginning of a turn-on sequence, the voltage at pin DESAT is forced to LOW level for the duration of the blanking time (defined in the respective 1EDI2002AS registers). Once the blanking time has elapsed, the voltage at pin DESAT is released and is compared to an internal reference voltage. Due to the additional decoupling capacitance (100nF), an additional "analogue" blanking time will be added corresponding to the charging of the capacitance through the internal pull-up resistance.
In case the measured voltage is higher than the configured internal threshold, a save turn-off sequence is initiated by the 1EDI2002AS device and the corresponding error flags and fault signals are activated.

For details regarding DESAT protection configuration please refer to the Infineon 1EDI2002AS datasheet [4].

### 5.3.3 Active clamping and additional gate-emitter components

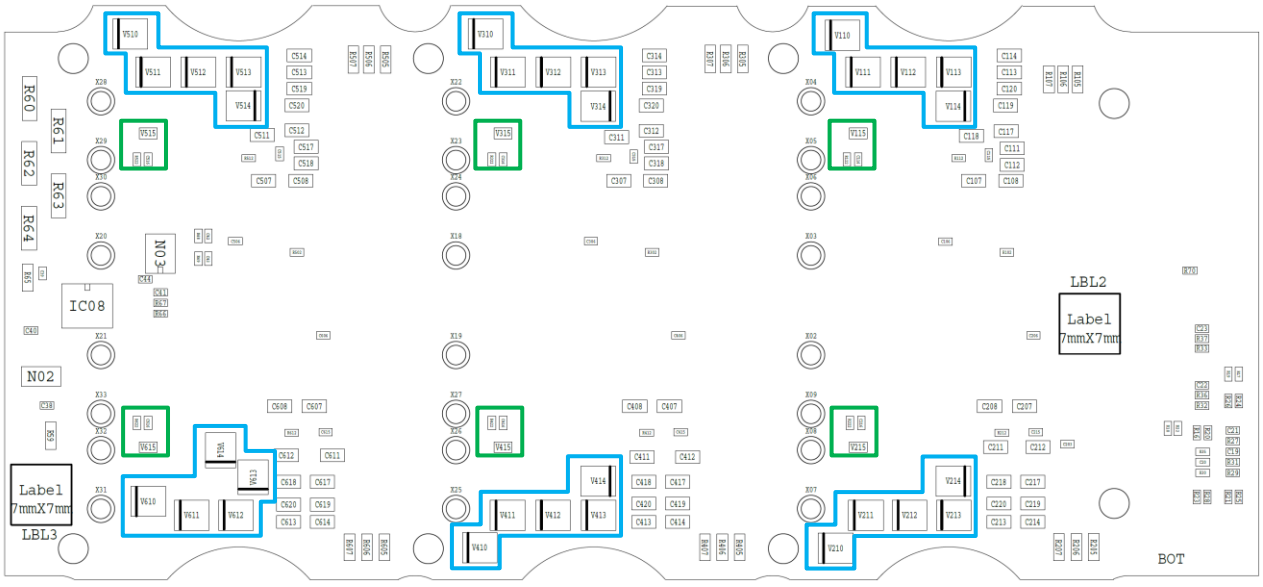
The Application Sample allows the user to implement an Active clamping feature on the Gate Driver Board. Figure 15 shows the schematic of the active clamping feature used in the Application Sample. The driver board offers five pads sized SMB (DO214AA) per IGBT (framed in blue in Figure 16) for placing TVS diodes (transient voltage suppressor diodes) on the PCB bottom side.
By factory setting the **active clamping diodes are NOT populated**.

**Figure 15: Active clamping schematics**




Besides the active clamping functionality every IGBT is protected by a RC network (10kΩ/10nF) between Gate and Emitter. Two clamping diodes connected from gate to +15V and -8V protects the gate from any unwanted transient voltages on the gate signal. The additional GE components are framed in green in Figure 16.

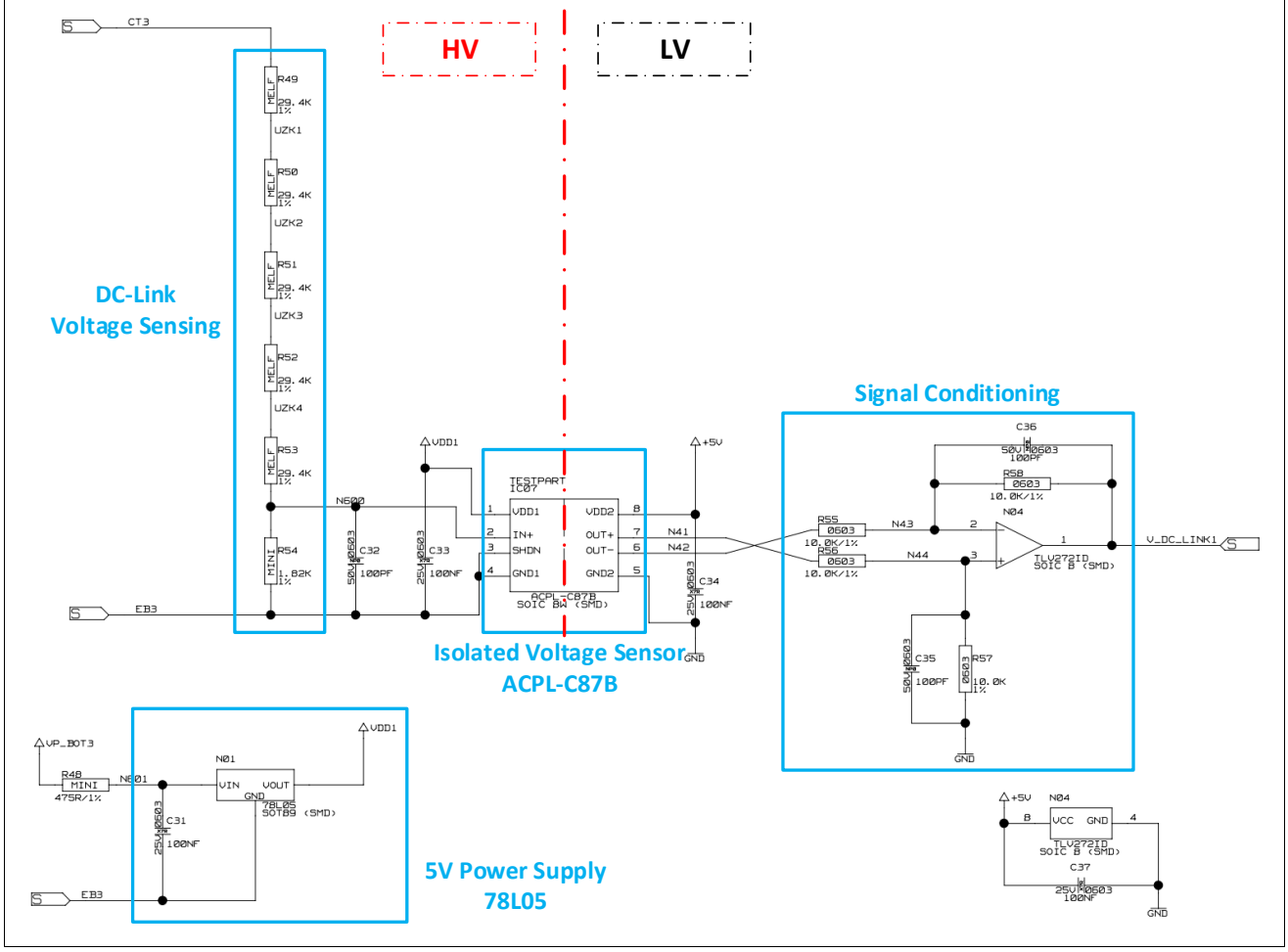
**Figure 16: Placement pads for the active clamping diodes**




## 5.4 DC-link voltage measurement

The Gate Driver Board comprises two (redundant) isolated DC-Link measurement circuits. Figure 17 shows the schematic of one of the two identical DC-Link measurement circuits.

**Figure 17: DC-link voltage measurement schematic (channel 1)**




The measurement is realized by a high impedance isolated voltage sensor (ACPL-C87B). The circuit measures the DC bus voltage via the auxiliary TOP-Collector (+DC potential) and BOT-Emitter (-DC potential) of phase W. The DC bus voltage is scaled down to the input voltage range of the voltage sensor by a resistive divider. The resistive divider uses the following values:

| Channel | Position | Package | Value 750V class | Value 1200V class |
|---|---|---|---|---|
| 1 | R49…R53 | 5x MELF (0207) | t.b.d | t.b.d |
| | R54 | MiniMELF (0204) | t.b.d | t.b.d |
| 2 | R60…R64 | 5x MELF (0207) | t.b.d | t.b.d |
| | R65 | MiniMELF (0204) | t.b.d | t.b.d |

Both isolated voltage sensors are powered by the 15V supply voltage of IGBT T6.
The differential output signal of the ACPL-C87 is converted to a single-ended analogue output signal via an op-amp converter. The output signals of both DC-Link measurement are connected to the X01 connector:

| Pin | Signal name | Description | Direction | Voltage Level |
|---|---|---|---|---|
| B21 | V_DC_LINK1 | DC-Link voltage measurement 1 | OUT | 0..5V analogue output |
| A22 | V_DC_LINK2 | DC-Link voltage measurement 2 | OUT | 0..5V analogue output |

Figure 18 and Figure 19 shows the relation between measured DC-Link voltage and the V_DC_LINKx analogue output signal on the X01 connector. There are different scalings for the different voltage classes (750V, 1200V).

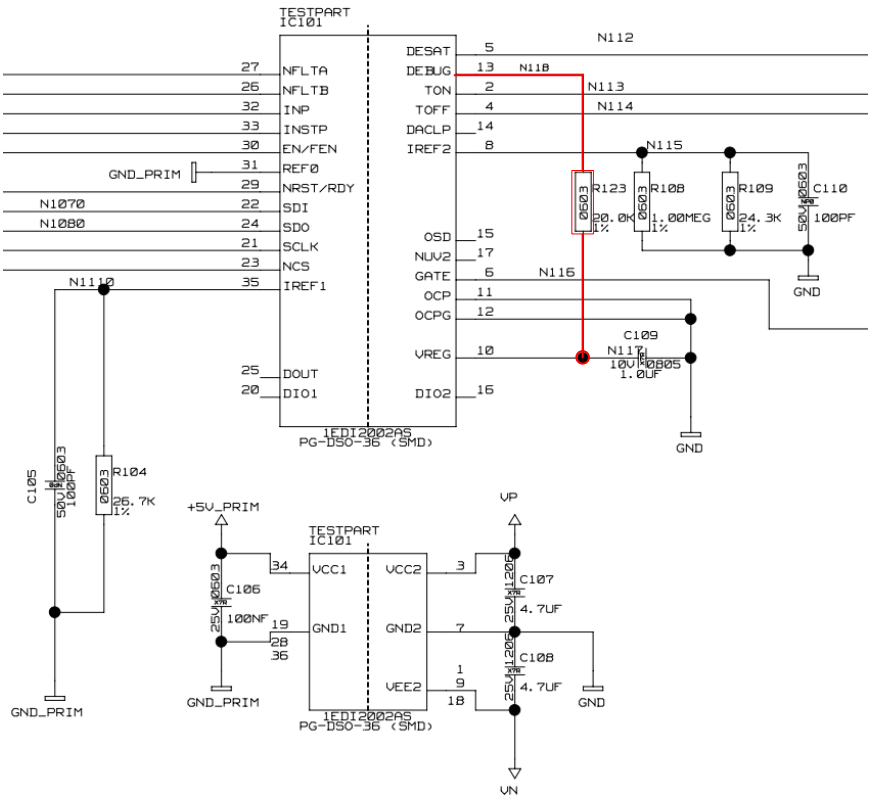
**Figure 18: DC-link voltage analogue output characteristic, 750V class, t.b.d.**

**Figure 19: DC-link voltage analogue output characteristic, 1200V class,t.b.d.**

### 5.5 Debug mode

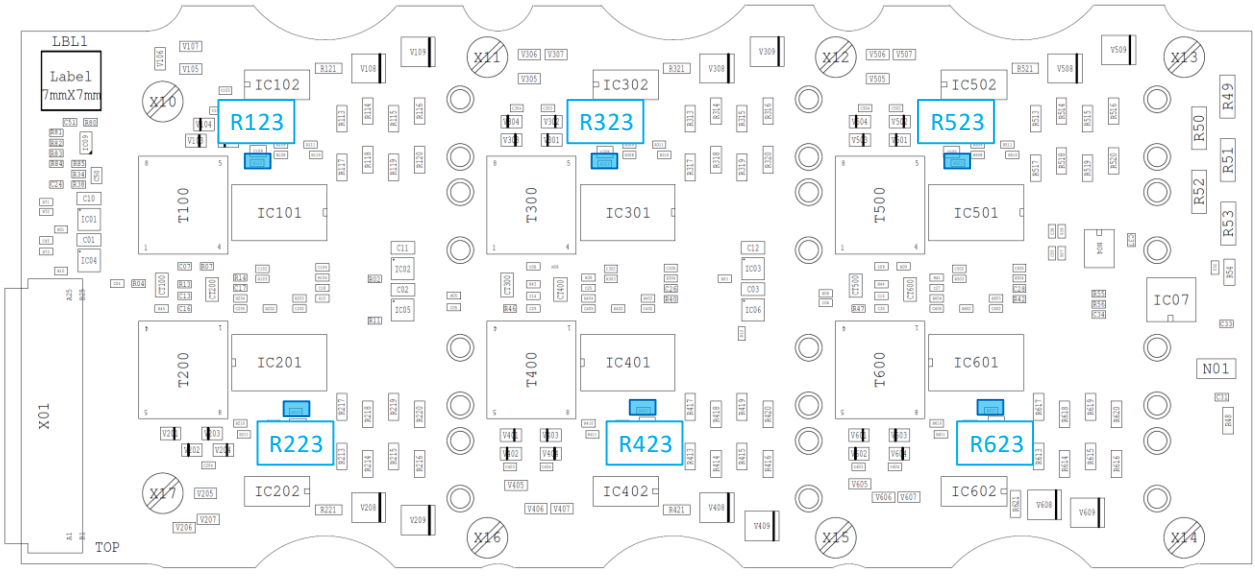
The DEBUG pin on the 1EDI2002AS Gate Driver gives the possibility to operate the device in the so-called Debug Mode. The goal of the Debug Mode is to operate the device without SPI interface. **This mode should be used for development purpose only and is not intended to be used in final applications.**

**Figure 20: Debug mode setting**




The Debug mode is activated by default on the Gate Driver Board. For changing the EICE Driver(s) into the standard (SPI-) mode, the resistors R123, R223, R323, R423, R523 and R623 need to be removed and the DEBUG pin must be left open. This 6 resistors are all located at the same position in relation to the driver IC as shown in Figure 21.

**Figure 21: Placement of the DEBUG resistors on PCB TOP side**



## 5.6 SPI interface

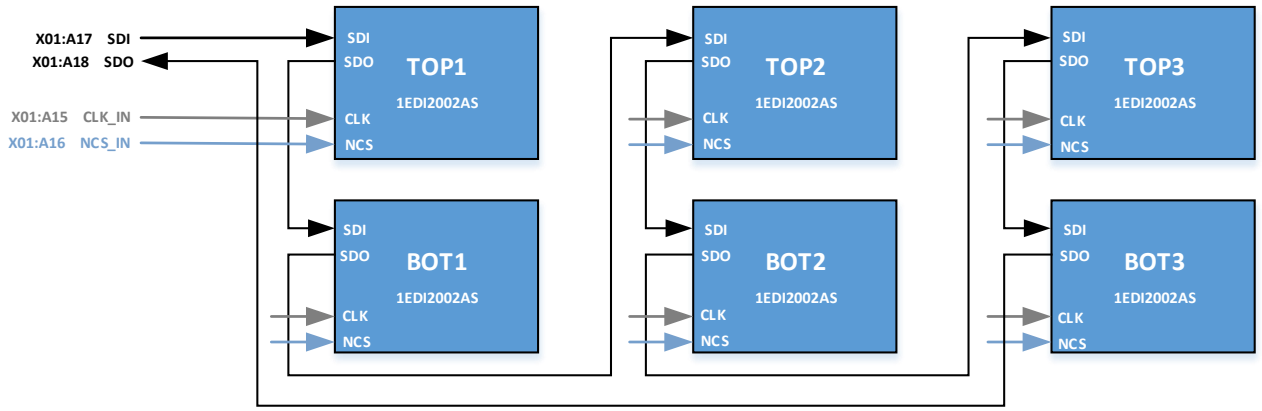
The 1EDI2002AS Gate Driver provides an SPI interface which allows a standardized bidirectional communication with a main microcontroller on the user side. The SPI interface of the 1EDI2002AS supports slave operation only.

The SPI interface relies on four communication signals:

- NCS: (Not) Chip Select
- SCLK: Serial Clock
- SDI: Serial Data In
- SDO: Serial Data Out

In order to simplify the PCB layout and reduce the number of pin on the user's main microcontroller a daisy chain topology was used as shown in Figure 22.

**Figure 22: SPI bus daisy chain topology**




In a regular SPI bus topology the SPI slaves are addressed separately by an individual (negative) chip select signal of each slave device. In a daisy chain topology all slaves are connected to the same (negative) chip select signal of the main microcontroller and are addressed simultaneously. In this topology all SPI slaves are connected in series via the SDO and SDI signals. At each rising edge of the SCLK signal (while NCS is active), the shift output register is serially shifted out by one bit on the SDO pin (MSB first). At each falling edge of the clock pulse, the data bit available at the input SDI is latched and serially shifted into the shift input register.

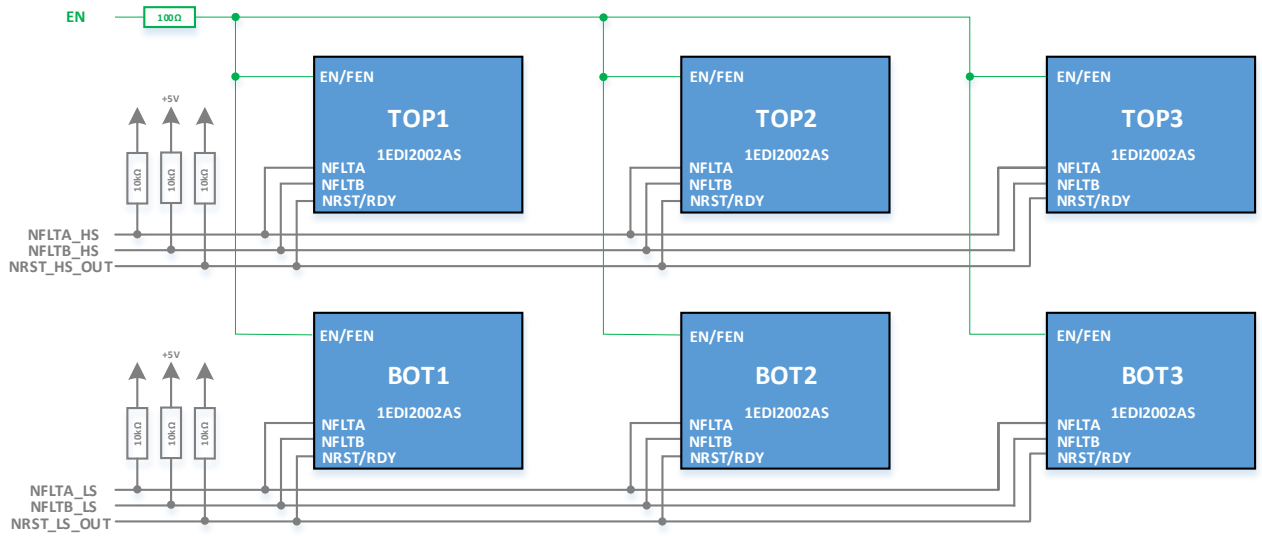
For detailed description of the SPI interface and SPI registers please refer to the 1EDI2002AS datasheet.

Please note that the 1EDI2002AS gate driver devices are configured for **Debug mode by factory setting**. In Debug Mode, the regular operation of the internal state machine is modified which allows operation without SPI interface. In order to configure the gate driver via SPI interface the 1EDI2002AS devices must be configured for normal operating mode. Please refer to chapter 5.5 for detailed information.

## 5.7 Failure management

Besides the SPI-Interface the 1EDI2002AS gate driver provides several feedback and control pins in order to allow the user a fast reaction on certain events in critical applications

**Figure 23: Reset and fault logic**




### 5.7.1 Fault logic

The 1EDI2002AS gate driver provides two Open-Drain output signals NFLTA and NFLTB in order to report major failure events (Event Class A or Event Class B) in a fast way to the users main controller. In case of an Error Event Class A the NFLTA signal is driven to LOW state, in case of an Error Event Class B the NFLTB signal is driven to LOW state respectively. In general the activation of signal NFLTA or NFLTB is linked to a state transition of the device's internal state machine.
For detailed information regarding error management and state transitions please refer to the 1EDI2002AS datasheet [4].

In order to reduce the number of pins on the gate driver interface the error signals NFLTA and NFLTB are summarized for the three high side switches (NFLTA_HS, NFLTB_HS) and for the three low side switches (NFLTA_LS, NFLTB_LS) respectively (Figure 23). If either one of the high side switches or one of the low side switches rises an error the respective sum signal (NFLTA_LS, NFLTB_LS) will be driven to LOW state.

### 5.7.2 Reset logic

The 1EDI2002AS gate driver provides a NRST/RDY signal which combines both Reset and Ready notification.
The activation of this signal is associated with Reset events of the gate driver. In case of a Reset event the signal NRST/RDY is driven to LOW state. A HIGH level on this pin indicates that the primary chip is functional and will bring the device in its default state. Therefore this signal is also used as a "ready notification".
For detailed information regarding Reset events and state transitions please refer to the 1EDI2002AS datasheet.

In order to reduce the number of pins on the gate driver interface the Reset signals NRST/RDY are summarized for the three high side switches (NRST_HS_OUT) and for the three low side switches (NRST_LS_OUT) respectively (Figure 23). If either one of the high side switches or one of the low side switches rises a Reset events the respective sum signal (NRST_HS_OUT, NRST_LS_OUT) will be driven to LOW state.

### 5.7.3 Enable logic

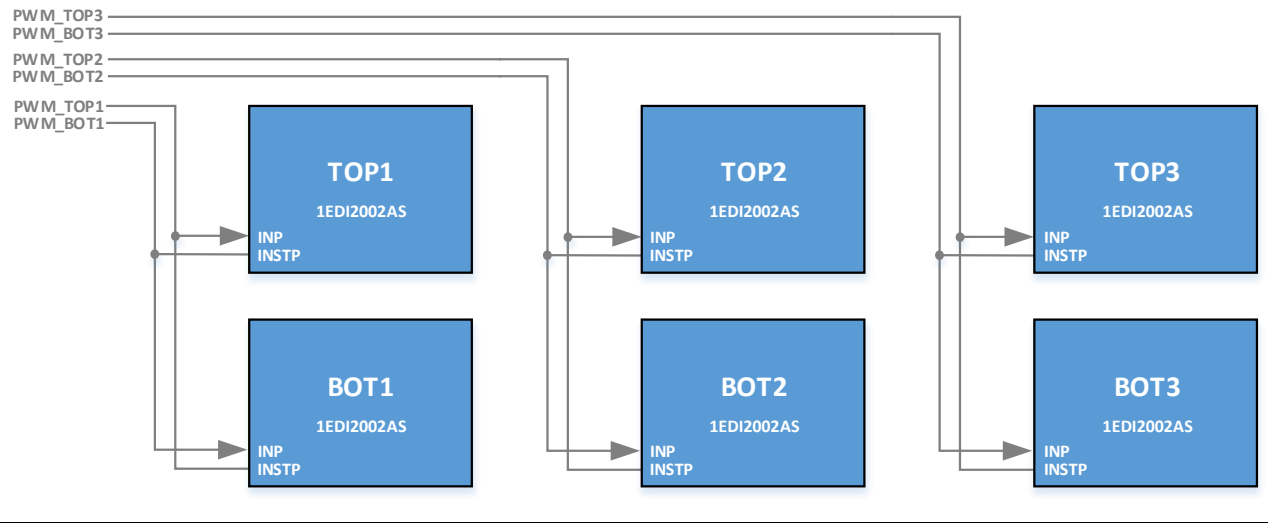
The 1EDI2002AS gate driver provides a EN/FEN signal which allows the logic on the primary side to have a direct control on the state of the device. A valid signal has to be provided on this pin. A valid to invalid transition of the signal on pin EN/FEN generates an Event Class A.
Pin EN/FEN should be driven actively by the user's main controller. In case this pin is floating, an internal weak pull-down resistor ensures that the signal is low.
For detailed information regarding Enable mode configuration please refer to the 1EDI2002AS datasheet [4].

In order to reduce the number of pins on the gate driver interface the Enable signals EN/FEN of all six switches are summarized to the enable signal EN (Figure 23). Controlling the EN pin on the gate driver interface will control all six switches simultaneously.

### 5.8 Shoot through protection

The 1EDI2002AS gate driver provides a Shoot through protection (STP-) function which prevents a simultaneous activation of the high- and low-side switches.

**Figure 24: Shoot through protection (STP)**




The input pin INSTP provides an input for the PWM signal of the driver's counterpart. With the implemented STP function, the low-side (resp. high-side) device is able to monitor the status of its high-side (resp. low-side) counterpart.
In case of an active low-side switch (HIGH signal on the INP pin) the activation of the respective high-side switch (HIGH signal on the INP pin) is inhibited (and vice versa). If a HIGH signal is received during the inhibition time, a failure event is detected. A minimum dead time is defined by the hardware of 1EDI2002AS gate driver and can be further adjusted via SPI interface.

For detailed information regarding STP error handling and delay configuration please refer to the 1EDI2002AS datasheet [4].

### 5.9 Temperature measurement

All eMPack IGBT modules come with an NTC-resistor for temperature measurement. The NTC is sintered onto the same DBC ceramic substrate near the IGBT and diode chips and reflects the actual case temperature. Every single half bridge has its own temperature sensor. Since the cooling conditions have a significant influence on the temperature distribution inside the eMPack module, it is necessary to evaluate the dependency between the temperatures of interest (e.g. chip temperature) and the signal from the integrated temperature sensor.

The temperature sensor has a nominal resistance of $R_{25}$=4.7kΩ at 25°C. The measuring current should be 1mA, a maximum value of 3mA must not be exceeded.

The mathematical approximation of the sensor resistance ($R_{NTC}$) as a function of temperature ($T_{DCB}$) is given by the following equation:

$$R_{NTC} = R_{25} \cdot exp\left[B_{25/85} \cdot \left(\frac{1}{T} - \frac{1}{298{,}15K}\right)\right]$$

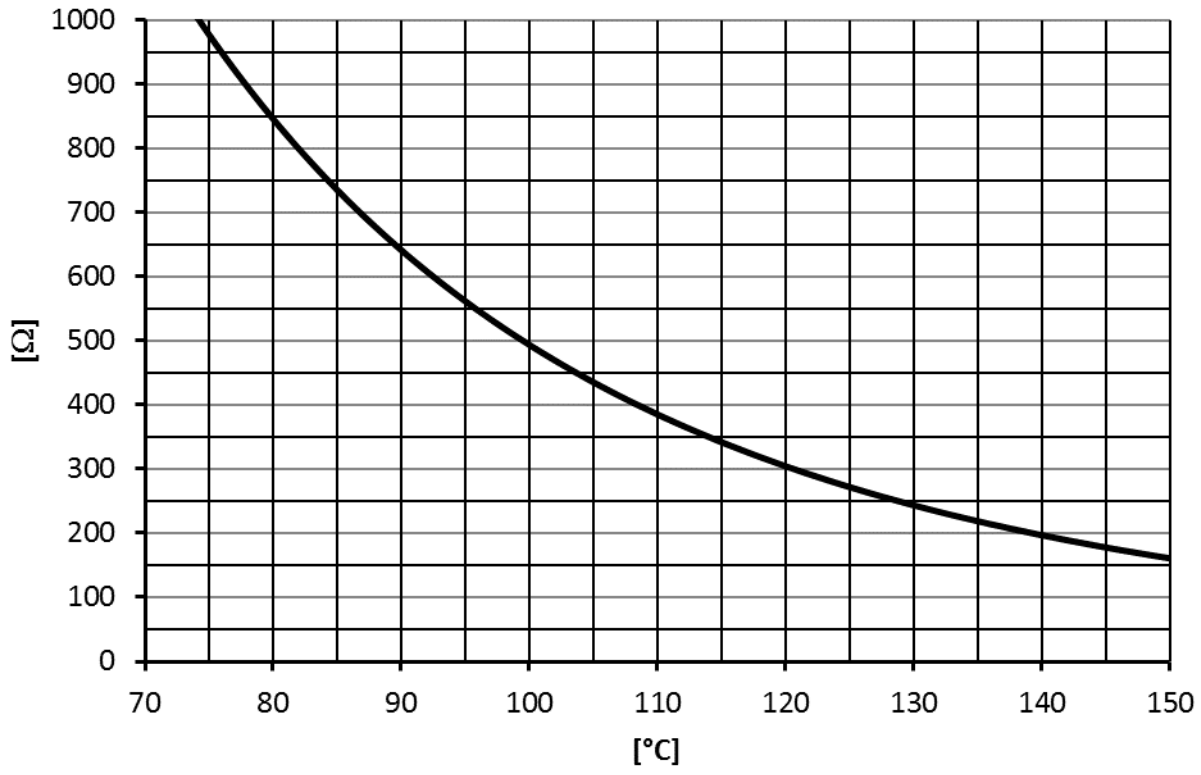
With

$R_{25}$: nominal resistance at nominal temperature ($T_{nom}$ = 25°C)
$B_{25/85}$: material constant
T: absolute operating temperature ($T_{DCB}$ + 273.15K)

Values $R_{25}$ and $B_{25/85}$ are given in the respective eMPack module datasheet.

Figure 25 shows an excerpt of the eMPack NTC characteristic, which includes the most interesting temperature range between 25°C and 150°C.

**Figure 25: eMPack NTC temperature sensor characteristic (excerpt)**



# 6. Electrical and Mechanical Characteristics

## 6.1 Absolute maximum ratings

With regard to the requirement specification the eMPack Application Kit allows for operation within the boundaries as stated in Table 13 and Table 14:

| **Table 13: Environmental ratings of the eMPack Application Kit** | |
|---|---|
| ambient temperature $T_a$ | 0°C to +40°C |
| IP rating | IP00 |
| Climate class operation | 3K3 |
| Pollution degree | PD2 |
| Installation altitude | ≤ 2000m above sea level |

| **Table 14: Absolute maximum ratings of the eMPack Application Kit** | | |
|---|---|---|
| | DC-Link Voltage ($V_{DC,max}$) | Gate Driver Board switching frequency ($f_{sw}$) |
| eMP1020MD075SC2SV1DPD | 600V | 16kHz |
| eMP780MD12SC2SV1DPD | 900V | 16kHz |
| eMP1080GD075ED2V1DPD | 600V | 16kHz |
| t.b.d. | t.b.d. | 16kHz |

Neglecting the above mentioned boundaries may lead to malfunction or damage of the Application Kit. All components are rated -40°C to +125°C, however, the Application Sample has not been tested beyond 0° to +40°C.

## 6.2 DC-link discharge

The eMPack Application Kit does neither comprise an active nor a passive discharge circuitry. **The DC-Link capacitor needs to be actively discharged by the user.**

## 6.3 Insulation system of the Gate Driver Board

For functional and safety purposes the gate driver board is separated into two insulated parts, the driver low voltage side (blue marked section in Figure 26 and Figure 27) which mainly consists of the X01 signal interface and analogue and digital signal conditioning circuits and the driver high voltage side (red marked sections in Figure 26 and Figure 27) which mainly consists of the gate driver, measurement and protection circuits. The insulation between primary and secondary side is realized by magnetic DC/DC converters and optical couplers.
For functional reasons the secondary side gate drivers are also separated into TOP and BOTTOM part by functional insulation barrier.

**Figure 26: Driver TOP side isolation barrier**

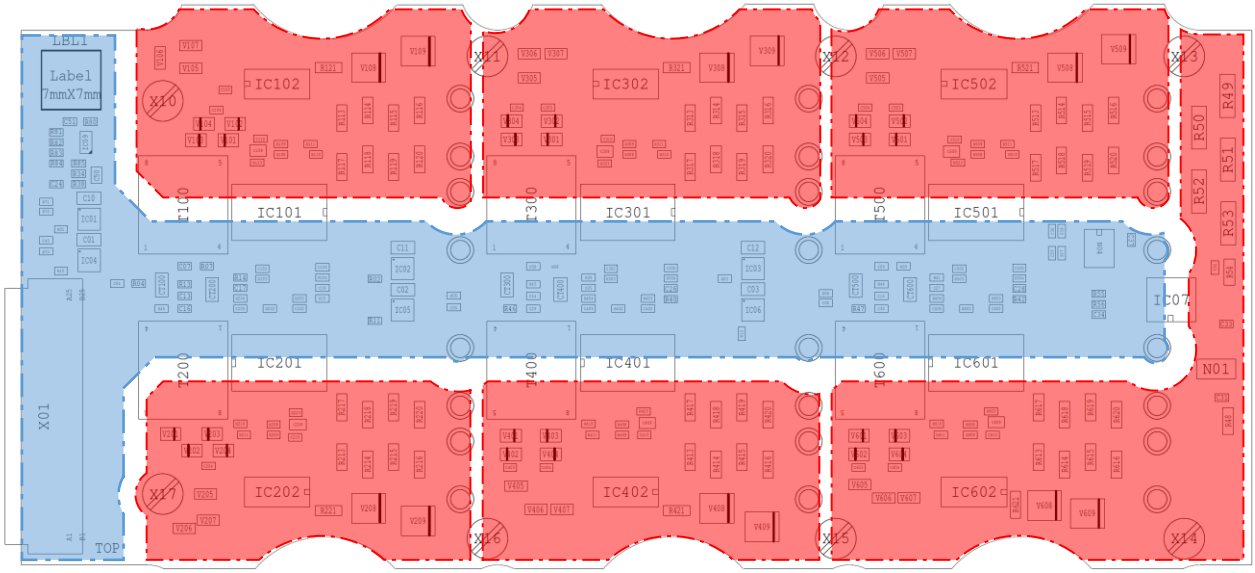
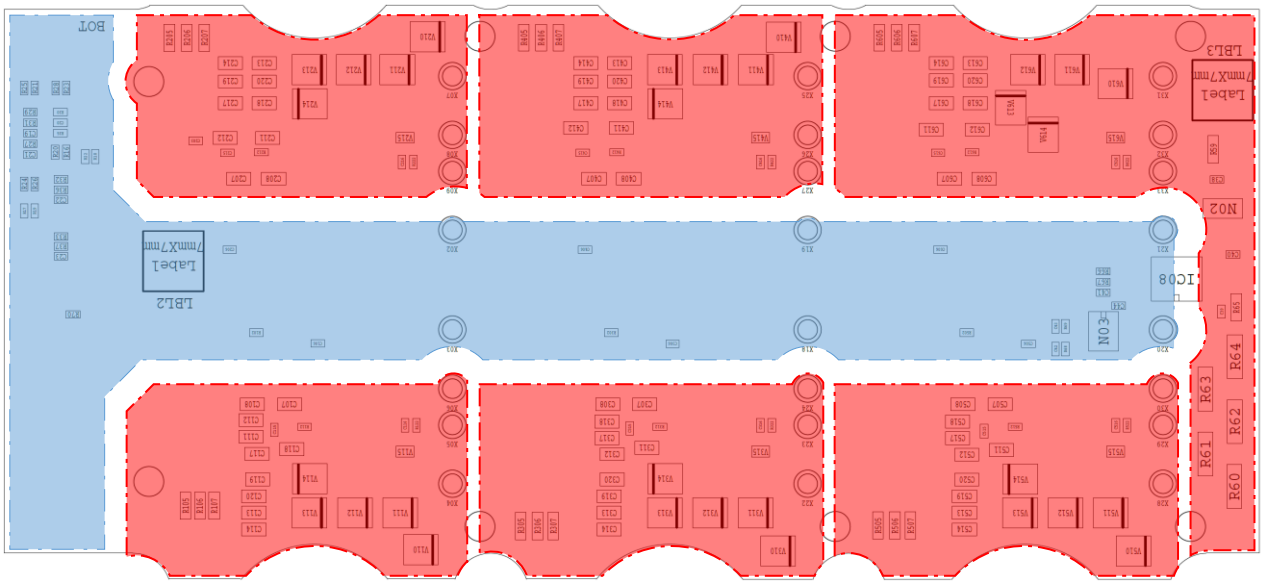



**Figure 27: Driver BOT side isolation barrier**



**Symbols and Terms**

| Letter Symbol | Term |
|---|---|
| AC | Alternating Current; output terminal of inverter |
| AWG | American Wire Gauge |
| BOT | Lower switch of halfbridge |
| DC- | Negative potential (terminal) of a direct voltage source |
| DC+ | Positive potential (terminal) of a direct voltage source |
| DCB | Direct copper bonded; ceramic substrate of power modules |
| DPD | Direct Pressed Die |
| ESD | Electrostatic Discharge |
| $f_{sw}$ | Switching frequency |
| GND | Ground |
| HV | High Voltage |
| IGBT | Insulated Gate Bipolar Transistor |
| $I_{R,max}$ | Maximum ripple current of DC-link capacitor |
| LV | Low Voltage |
| NTC | Temperature sensor with negative temperature coefficient |
| PCB | Printed Circuit Board |
| PSU | Power Supply Unit |
| $R_{Goff}$ | External gate series resistor at switch-off |
| $R_{Gon}$ | External gate series resistor at switch-on |
| Si | Silicon |
| SiC | Silicon-Carbide |
| SPI | Serial Peripheral Interface |
| STP | Shoot Trough Protection |
| $T_a$ | Ambient temperature |
| TOP | Upper switch of halfbridge |
| TVS | Transient voltage suppressor |
| $V_{AC}$ | Output voltage of inverter |
| $V_{CE}$ | Collector-emitter voltage |
| $V_{DC}$ | Total supply voltage between DC+ and DC- |

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

## References

[1] www.SEMIKRON.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3
[3] I. Bogen, "eMPack Power Module", SEMIKRON Mounting Instruction - rev01, 2020
[4] Infineon Technologies AG, "EiceDRIVER™ SIL 1EDI2002AS", Infineon Datasheet – Rev.3.1, Munich, 30.07.2015

## IMPORTANT INFORMATION AND WARNINGS



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