SEMIKRON
innovation+service

Technical Explanation
SEMIPACK®

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1. Introduction

As the first insulated power module in the world, SEMIPACK 1 was invented in 1974 by SEMIKRON. Now SEMIPACK has already become a complete family with different case sizes and configurations. SEMIPACK products have the widest output current range up to 1360 A, reverse voltage from 600V to 2200V. At present, there are two production locations for SEMIPACK products: SKSK (Slovakia) has the focus at soldered bonded and pressure contact modules, whereas in SKI (Italy) fast diode modules and special types are manufactured.

1.1 Features

Semiconductor chips soldered onto ceramic insulated metal baseplate (SEMIPACK 0…2 and a part of SEMIPACK 3 modules) or pressure contact modules (SEMIPACK 3, 4, 5 and 6) with very high load cycle capability.

The SEMIPACK product family consists of thyristor modules (single and dual), rectifier diode modules (single and dual), thyristor/rectifier diode modules and fast diode modules (single and dual). The corresponding current rating and voltage class ranges are given below:

- thyristor modules: current ratings from 15A to 800A, voltage classes from 600V to 2200V.
- rectifier diode modules: current ratings from 15A to 1360A, voltage classes from 800V to 2200V.
- fast diode modules: current ratings from 40A to 308A, voltage classes from 600V to 1700V.

Optimum heat transfer to the heat sink is ensured by using ceramic insulated metal baseplate with Al_2O_3 (SEMIPACK 0,1,2 and part of SEMIPACK 3) or AlN (SEMIPACK 3 – 6) insulating substrate.

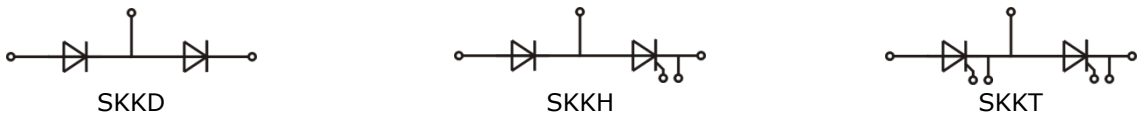
For SEMIPACK 1 and 2, several generations with variations of internal and external layouts are in production.

All SEMIPACK modules are UL recognized (file no. E 63 532).

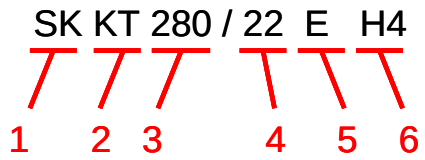
1.2 Topologies

SEMIPACK products are available as single component elements or double packs with internal, functional interconnection. Available topologies are shown below:

Figure 1: SEMIPACK standard topologies



1.3 Type designation



1: SEMIKRON component
2: Topology of internal connection, please refer to *Fig.1*
3: Rated current (I_{TAV} [A])
4: Voltage class (V_{RRM}[V])
5: dv/dt class
D: 500 V/µs
E: 1000 V/µs
G: 2000 V/µs
6: Option, where applicable, e.g. H4 stands for V_{isol} = 4.8kV

1.4 Typical applications

- Soft starter for induction motors
- Line rectifier for transistorized AC motor controllers
- DC motor control (e.g. for machine tools)
- Field supply for DC motors
- Temperature control (e.g. for ovens, chemical processes)
- Professional light dimming (studios, theatres)
- UPS

2. Mechanical details of SEMIPACK products

2.1 SEMIPACK housings

Figure 2: SEMIPACK housings

SEMIPACK 0

SEMIPACK 1.5

SEMIPACK 1.6

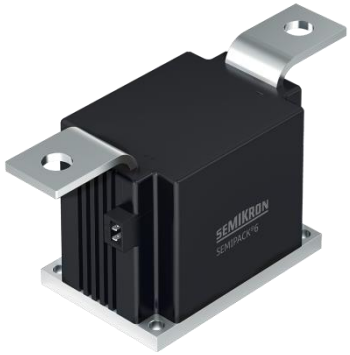
SEMIPACK 2

SEMIPACK 3 bonded

SEMIPACK 3
pressure contact

SEMIPACK 4

SEMIPACK 5



SEMIPACK 6

SEMIPACK has 7 different housing sizes, from SEMIPACK 0 to SEMIPACK 6. Below are main dimensions of different housings:

Table 1: Main dimensions of different SEMIPACK housing sizes

	Length [mm]	Width [mm]	Height [mm]
SEMIPACK 0	61	21	25
SEMIPACK 1	93	20	30 (29.5*)
SEMIPACK 2	94	34	30
SEMIPACK 3	115	51	54
SEMIPACK 4	101	50	52
SEMIPACK 5	150	60	52
SEMIPACK 6	176	70	90

*SEMIPACK1 3rd generation

For SEMIPACK products, general tolerance of catalogue drawings is ±0.5mm, if not stated differently.

2.2 Creepage and clearance distance

All SEMIPACK thyristor and diode modules comply with the required creepage and clearance distances in accordance with DIN EN 50178.

Table 2: Creepage and clearance distances for SEMIPACK

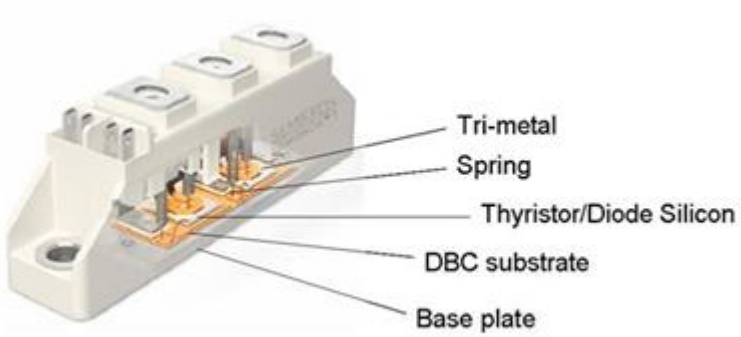
[mm]	Clearance distance		Creepage distance	
Terminal	1-2	2-3	1-2	2-3
SEMIPACK 1.5	10	10	14	14
SEMIPACK 1.6	10	10	15	15
SEMIPACK 2	9	9	14	14
SEMIPACK 3 bonded	37	17	37	17
SEMIPACK pressure contact	37	17	37	17
SEMIPACK 4	19	--	19	--
SEMIPACK 5	19	25	23	28
SEMIPACK 6	84	--	84	--

2.3 Different internal constructions

In order to satisfy various market demands, SEMIPACK family has three different internal constructions:
- soldered construction (SEMIPACK 1)
- bonded construction (SEMIPACK 0, 2, 3)
- pressure contact construction (SEMIPACK 3, 4, 5, 6)

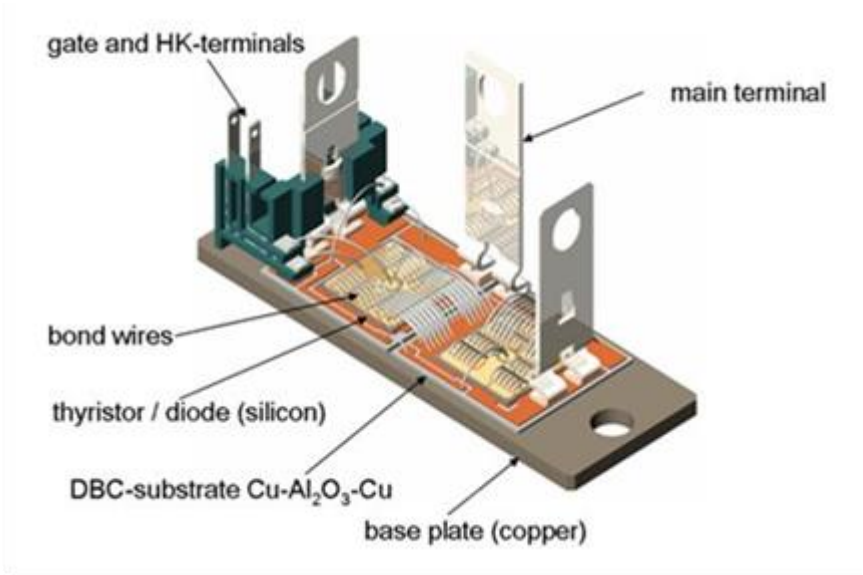
Soldered construction - the contact is established by solder layers.

Figure 3: SEMIPACK 1 soldered construction



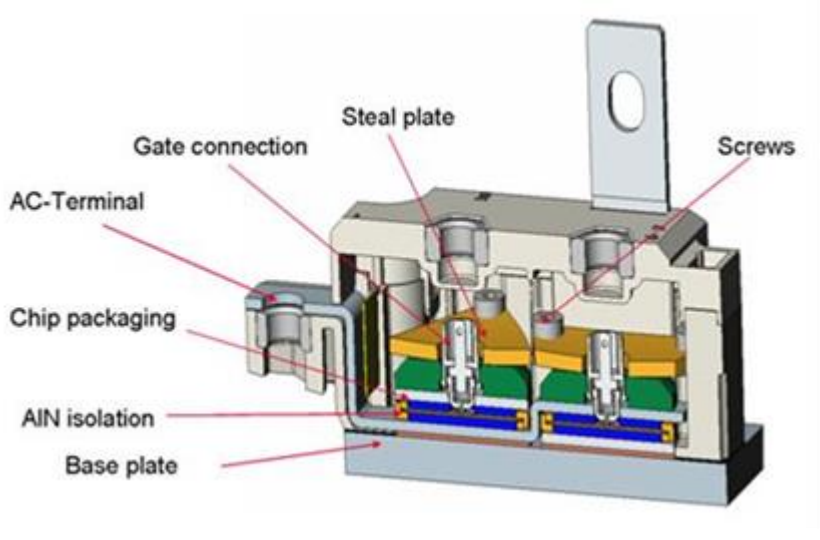
Bonded construction - the connection between top electrode of the chips and DBCs is realized by bond wires.

Figure 4: SEMIPACK 2 bonded construction



Pressure construction - the contact is established by pressure, solder free assembly.

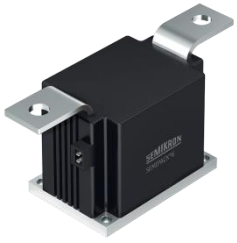
Figure 5: SEMIPACK 3 pressure contact construction



2.4 Mechanical samples

Following SEMIPACK mechanical samples can be ordered. Corresponding Item-Numbers are given below:

Table 3: Item numbers of SEMIPACK mechanical samples

Item Number	Type	Internal construction	Case picture (not to scale)
07891011	SEMIPACK 1.5	soldered	
07890100	SEMIPACK 1.6	soldered	
07890098	SEMIPACK 2	bonded	
07890096	SEMIPACK 3	bonded	
07898690	SEMIPACK 3	pressure contact	
07890094	SEMIPACK 4	pressure contact	
07898785	SEMIPACK 5	pressure contact	
07290040	SEMIPACK 6	pressure contact	

3. Explanation of parameters

3.1 Measuring of thermal resistance $R_{th(j-c)}$ and $R_{th(c-s)}$

The definition for thermal resistance R_{th} is the difference between two defined temperatures divided by the power loss P which gives rise to the temperature difference under steady state conditions:

$$R_{th(1-2)} = \frac{\Delta T}{P_V} = \frac{T_1 - T_2}{P_V} \qquad (3\text{-}1)$$

Depending upon the choice of the two temperatures the following thermal resistances can be distinguished:

- thermal resistance junction to case $R_{th(j-c)}$,
- thermal resistance case to heatsink $R_{th(c-s)}$,
- thermal resistance heatsink to ambient $R_{th(s-a)}$,
- thermal resistance junction to ambient $R_{th(j-a)}$, etc.

The data sheet values for the thermal resistances are based on measured values. As can be seen in equation (3-1), the temperature difference ΔT has a major influence on the R_{th} value. As a result, the reference points and the measurement methods will have a major influence too.
SEMIKRON measures the $R_{th(j-c)}$ and $R_{th(c-s)}$ using method A shown in Figure 6: Method A as used for SEMIPACK, location of reference points for Rth measurement. This means the reference points are as follows:

For $R_{th(j-c)}$ they are a virtual junction of the chip (T_j) and the bottom side of the module (T_c), measured directly underneath the chip via a drill hole in the heat sink. Reference point 1, in Figure 6: Method A as used for SEMIPACK, location of reference points for Rth measurement.

For $R_{th(c-s)}$ once again the bottom side of the module (T_c) is measured as described above. The heat sink temperature T_s is measured on the top of the heat sink surface as close to the chip as possible.

Figure 6: Method A as used for SEMIPACK, location of reference points for Rth measurement

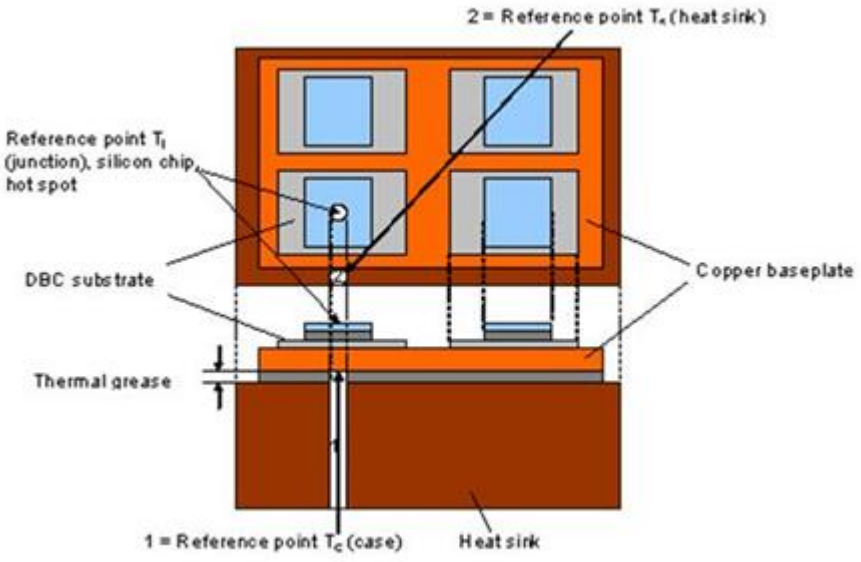
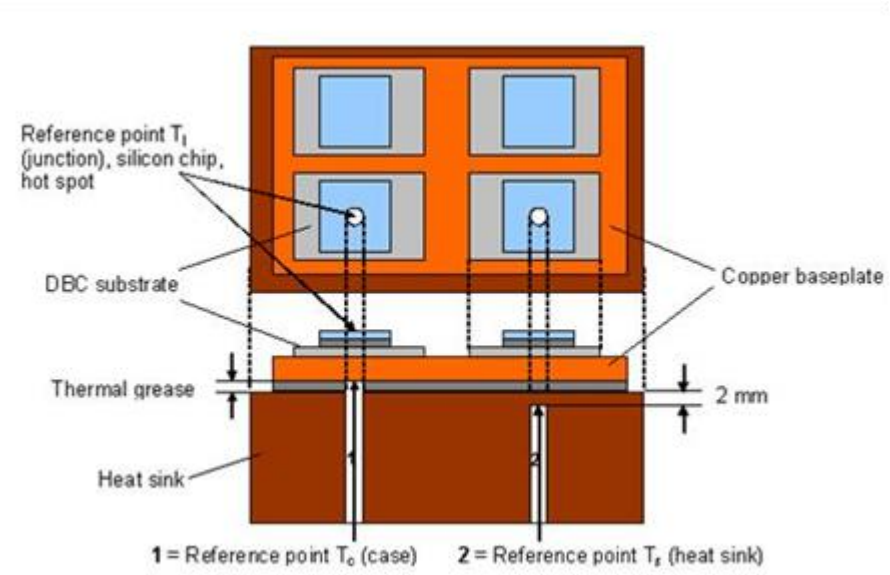


Figure 7: Method B, location of reference points for Rth measurement



As explained above, the measurement method and the reference points have a significant influence on the R_{th} value. Some competitors use method B, as shown in Figure 7: Method B, location of reference points for Rth measurement. The main difference is the second reference point for the measurement of $R_{th(c-s)}$. See reference point 2 in Figure 7: Method B, location of reference points for Rth measurement. This reference point is very close to the bottom side of the module inside the heat sink, i.e. in a drill hole. Due to the temperature distribution inside the heat sink (as shown in Figure 8: Thermal distribution and positions of different reference points for Tj, Tc, Ts and Ta for the methods A and B), the temperature difference ΔT (= T_c-T_s) is very small, meaning that $R_{th(c-s)}$ will be very small, too.

Figure 8: Thermal distribution and positions of different reference points for Tj, Tc, Ts and Ta for the methods A and B shows the temperature distribution and the location of the reference points for the different measurement methods. If equation (3-1) is taken into consideration, it is clear that $R_{th(c-s)}$ in method B must be smaller. That said, the reduction in $R_{th(c-s)}$ must ultimately be added to $R_{th(s-a)}$ (see Figure 9: Comparison of the resulting Rth values for the different methods), meaning that at least the thermal resistance $R_{th(j-a)}$ between junction and the ambient turns out to be the same, regardless of what measurement method is used.

Figure 8: Thermal distribution and positions of different reference points for Tj, Tc, Ts and Ta for the methods A and B

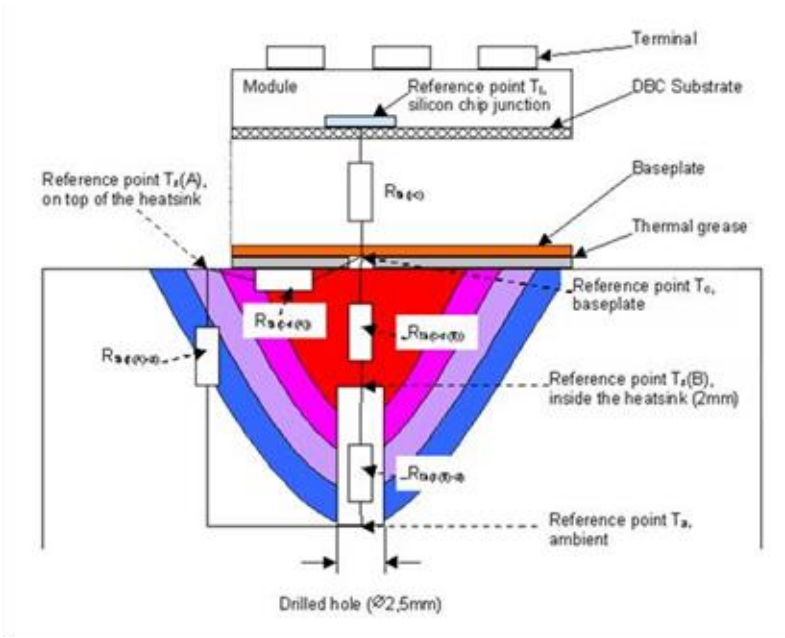
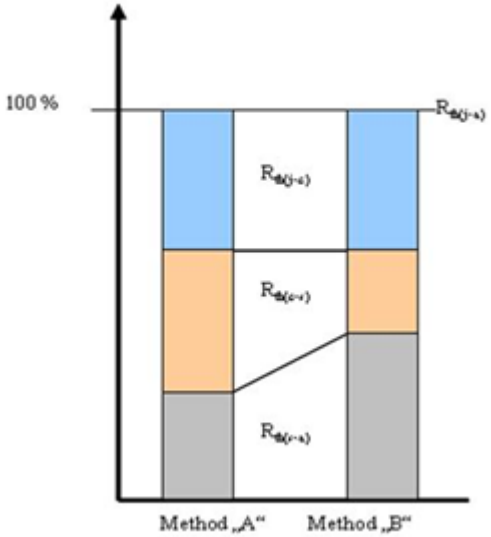


Figure 9: Comparison of the resulting Rth values for the different methods



For further information on the measurement of thermal resistances and understanding of datasheet values please refer to:

- M. Freyberg, U. Scheuermann, "*Measuring Thermal Resistance of Power Modules*"; PCIM Europe, May, 2003
- Dr. Arendt Wintrich, "Comparing the Incomparable"; Bodo's Power Systems® March 2011

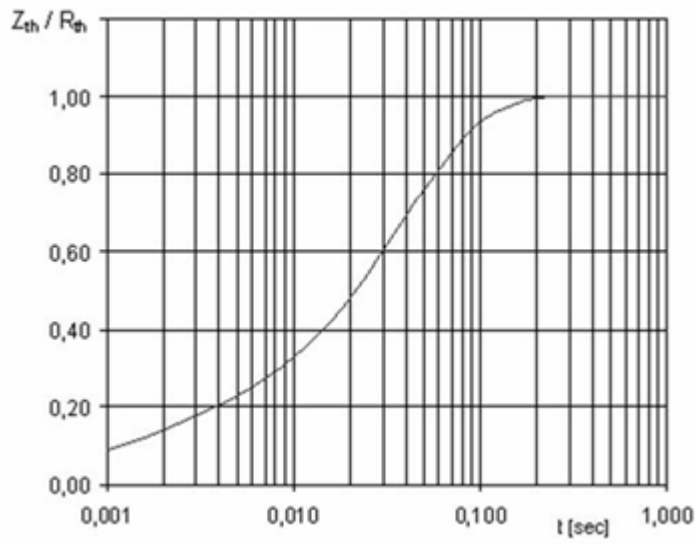
3.2 Transient thermal impedance

When switching on a "cold" module, the thermal resistance R_{th} appears smaller than the static value as given in the data sheets. This phenomenon occurs due to the internal thermal capacities of the package.

These thermal capacities are "uncharged" and will be charged with the heating energy resulting from the losses during operation. In the course of this charging process the R_{th} value seems to increase. During this time it is therefore called transient thermal impedance Z_{th}. When all thermal capacities are charged and the heating energy has to be emitted to the ambience, the transient thermal resistance Z_{th} has reached static data sheet value R_{th}.

The advantage of this behaviour is the short-term overload capability of the power module.

Figure 10: Example of the transient thermal impedance junction to case



During SEMIKRON's module qualification process the transient thermal behaviour is measured. On the basis of this measurement mathematical model is derived, resulting in the following equation (3-2):

$$Z_{th}(t) = R_1\left(1 - e^{\frac{-t}{\tau_1}}\right) + R_2\left(1 - e^{\frac{-t}{\tau_2}}\right) + \ldots + R_n\left(1 - e^{\frac{-t}{\tau_n}}\right) \qquad (3\text{-}2)$$

For SEMIPACK modules coefficients R_n, τ_n are available on request.

3.3 Explanation of electrical parameters

The terms in [ ] apply for thyristors only.

3.3.1 Insulation voltage V_{isol}

The insulation voltage of SEMIPACK® modules is a guaranteed value for the insulation between the terminals and the base plate. The limiting value of V_{rms} as specified in the data sheet for 1s is subject to 100% production testing.
All terminals - including the gate connections - must be interconnected during dielectric testing. All specifications for the final product's dielectric test voltage are described in the IEC publications IEC 60146-1-1 and EN 60146-1-1 (VDE 0558-11), EN 50 178 (VDE 0160), as well as in UL 1557. For railway applications, for instance, please refer to the specifications of the IEC 61287-1 standard.

3.3.2 Non-repetitive peak reverse voltage V_{RSM}; [Non-repetitive peak off-state voltage V_{DSM}]

Maximum permissible value for non-repetitive, occasional transient peak voltages at 25°C.

3.3.3 Repetitive peak reverse and off-state voltages [V_{DRM}] and V_{RRM}

Maximum permissible value for repetitive transient off-state and reverse voltages at 25°C.

3.3.4 Direct reverse voltages V_R for continuous duty

Maximum permissible direct reverse voltage for stationary operation for diodes (V_R) [or thyristors (V_D, V_R)]. This value is 0.7 V_{RRM} [0.7 V_{DRM}].

3.3.5 Mean forward [on-state] current I_{FAV}, [I_{TAV}]

The symbols I_{FAV}, [I_{TAV}] are used to refer to both the mean current values in general and the current limits. The limiting values are absolute maximum continuous values for the on-state current load of a diode [thyristor] for a given current waveform and given cooling conditions (e.g. case temperature T_c). At this current value, the maximum permissible junction temperature is reached, with no margins for overload or worst-case reserves. The recommended maximum continuous current is therefore approximately 0.8 I_{TAV} . For operation frequencies of between 40 Hz and 200 Hz the maximum mean on-state current can be taken from Fig. 1 of the datasheet. If standard diodes and thyristors (diodes/thyristors for line application) are operated at frequencies of between 200 Hz and 500 Hz, further current reductions should be carried out to compensate for the switching losses that are no longer negligible.

3.3.6 RMS forward [on-state] current I_{FRMS}, [I_{TRMS}]

The symbols I_{FRMS}, [I_{TRMS}] are used to refer to both the mean current values and the current limits. The limiting values are absolute maximum values for the continuous on-state current for any chosen current waveform and cooling conditions.

3.3.7 Surge forward [on-state] current I_{FSM} [I_{TSM}]

Peak value for a surge current in the form of a single sinusoidal half wave which lasts for 10 ms. After occasional current surges with current values up to the given surge forward current, the diode [thyristor] can withstand the reverse voltages specified in Fig. 8 or Fig. 16 of the datasheets.

3.3.8 Surge current characteristics $I_{F(OV)}$, [$I_{T(OV)}$]

Peak values for full or part sinusoidal half wave currents lasting between 1 ms and 10 ms or for sequential sinusoidal half wave currents with a maximum duration of 10 ms, permissible under fault conditions only, i.e. the diode [thyristor] may only be subjected to this value occasionally; the controllability of a thyristor may be lost during overload. The overload current depends on the off-state voltage value across the component (cf. Fig. 8 or Fig. 16 of the datasheets).

3.3.9 i^2t value

This value is given to assist in the selection of suitable fuses to provide protection against damage caused by short circuits and is given for junction temperatures of 25°C and 125°C. The i^2 t value of the fuse for the intended input voltage and the prospective short circuit in the device must be lower than the i^2t of the diode [thyristor] for t = 10 ms. When the operating temperature increases, the i^2t value of the fuse falls more rapidly than the i^2 t value of the diode [thyristor], a comparison between the i^2t of the diode (thyristor) for 25°C and the i^2t value of the (unloaded) fuse is generally sufficient.

The i^2t value is calculated from the surge on-state current I_{TSM} using the equation:

$$\int_0^{t_{hw}} i_{TS}^2 dt = I_{TSM}^2 \cdot \frac{t_{hw}}{2} \qquad (3\text{-}3)$$

Where t_{hw} is the duration of the half sinewave for which I_{TSM} has been specified. Thus at 50 Hz $t_{hw}/2$ = 0,005 s. i^2t has practically the same value for 60 as for 50 Hz since the 10% higher I_{TSM} is balanced out by the lower value for t_{hw} : $1.1^2 \cdot 8.3 \approx 10$.

3.3.10 [Critical rate of rise of on-state current $(di/dt)_{cr}$]

Immediately after the thyristor has been triggered, only part of the chips conducts the current flow, meaning that the rate rise of the on-state current has to be limited. The critical values specified apply to the following conditions: repetitive loads of between 50 and 60 Hz; a peak current value corresponding to the peak value of the permissible on-state current for sinusoidal half waves; a gate trigger current that is five times the peak trigger current with a rate of rise of at least 1 A/µs. The critical rate of rise for on-state current falls as the frequency increases, but rises as the peak on-state current decreases. For this reason, for frequencies > 60 Hz and pulses with a high rate of rise of current, the peak on-state current must be reduced to values below those given in the datasheets.

3.3.11 [Critical rate of rise of off-state voltage $(dv/dt)_{cr}$]

The values specified apply to an exponential increase in off-state voltage to 0.66 V_{DRM}. If these values are exceeded, the thyristor can break over and self-trigger.

3.3.12 Direct reverse [off-state] current I_{RD} [I_{DD}]

Maximum reverse [off-state] current for the given temperature and maximum voltage. This value depends exponentially on the temperature.

3.3.13 Direct forward [on-state] voltage V_F [V_T]

Maximum forward voltage across the main terminals for a given current at 25 °C.

3.3.14 Threshold voltage $V_{(TO)}$ [$V_{T(TO)}$] and forward [on-state] slope resistance r_T

These two values define the forward characteristics (upper value limit) and are used to calculate the instantaneous value of the forward power dissipation P_F [P_T] or the mean forward power dissipation P_{FAV} [P_{TAV}]:

$P_{F[T]} = V_{T(TO)} * I_{F[T]} + r_T * i^2_{F[T]}$
$P_{F[T]AV} = V_{T(TO)} * I_{F[T]AV} + r_T * I^2_{F[T]RMS}$
$I^2_{F[T]RMS} / I^2_{F[T]AV} = 360° / \Theta$
for square-wave pulses

$I^2_{F[T]RMS} / I^2_{F[T]AV} = 2.5$ or
$I^2_{F[T]RMS} / I^2_{F[T]AV} = (\pi/2)^2 * 180° / \Theta$
for [part] sinusoidal half waves

Θ: Current flow angle
$i_{F[T]}$: Instantaneous forward current value
$I_{F[T]RMS}$: RMS forward [on-state] current
$I_{F[T]AV}$: Mean forward [on-state] current

3.3.15 [Latching current I_L]

Minimum anode current, which at the end of a triggering pulse lasting 10 µs will hold the thyristor in its on-state. The values specified apply to the triggering conditions stipulated in the section on "Critical rate of rise of on-state current".

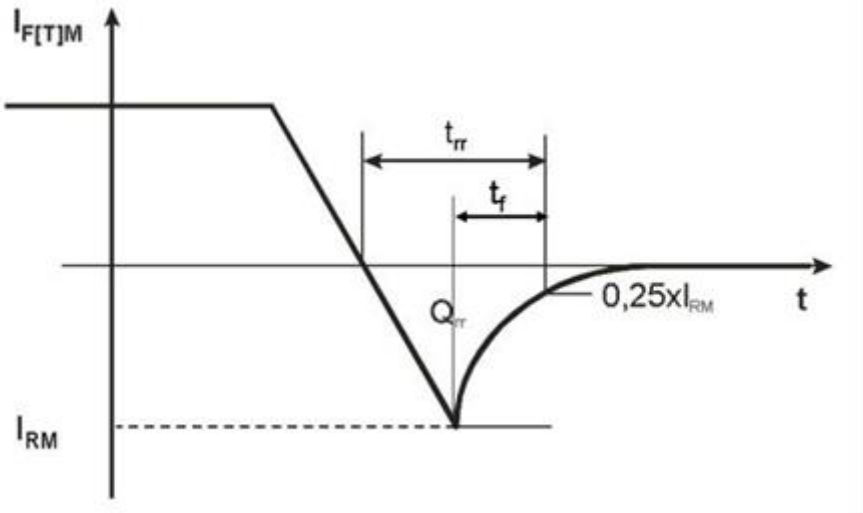
3.3.16 [Holding current I_H]

Minimum anode current which will hold the thyristor in its on-state at a temperature of 25°C. If the thyristor is switched on at temperatures below 25°C, the values specified may be exceeded.

3.3.17 Recovery charge Q_{rr}

Q_{rr} is the total charge which flows through the main circuit (current-time area) during commutation against the reverse recovery time t_{rr}. The corresponding characteristic in the datasheet shows this value's dependence on the forward current threshold value I_{FM} [I_{TM}] before commutation, as well as the forward current rate of fall di/dt (cf. Fig. 1 of the datasheet).

Figure 11: Current curve during diode/thyristor turn-off



The following relations exist between t_{rr}, Q_{rr}, the current fall time t_f and the peak reverse recovery current I_{RM} (cf. Fig. 1 of the datasheet):

$t_{rr} = I_{RM} / (- di_{F[T]}/dt) + t_f$
$t_{rr} = SQR (2 * Q_{rr} / (- di_{F[T]}/dt) + t_f^2 / 4) + t_f / 2$
$I_{RM} = 2 * Q_{rr} / t_{rr}$
$I_{RM} = SQR (2 * Q_{rr} * (- di_{F[T]}/dt) + t_f^2 / 4 * (- di_{F[T]}/dt)^2) - t_f / 2 * (- di_{F[T]}/dt)$

If the fall rate of the forward current I_F [I_T] is very low, t_f will be small in comparison to t_{rr} and the equations can be simplified as follows:
$t_{rr} = SQR (2 * Q_{rr} / (- di_{F[T]}/dt))$
$I_{RM} = SQR (2 * Q_{rr} * (- di_{F[T]}/dt))$

3.3.18 [Circuit commutated turn-off time t_q]

The circuit commutated turn-off time lies in the range of several hundred µs and constitutes the time required for a thyristor to discharge to allow it to take on forward voltage again. This value is defined as the time that elapses between zero crossing of the commutation voltage and the earliest possible load with off-state voltage. In the case of thyristors for phase-commutated converters and a.c. converters, the circuit commutated turn-off time is usually of no significance. For this reason, the datasheets contain typical values only, and no guarantee is given for these values.

3.3.19 [Gate trigger voltage V_{GT} and Gate trigger current I_{GT}]

Minimum values for square-wave triggering pulses lasting longer than 100 µs or for d.c. with 6 V applied to the main terminals. These values will increase if the triggering pulses last for less than 100 µs. For 10 µs, for instance, the gate trigger current I_{GT} would increase by a factor of between 1.4 and 2. Firing circuits should therefore be arranged in such a way that trigger current values are 4 to 5 times larger than I_{GT}. If the thyristor is loaded with reverse blocking voltage, no trigger voltage may be applied to the gate in order to avoid a non-permissible increase in off-state power losses and the formation of hot spots on the thyristor chip.

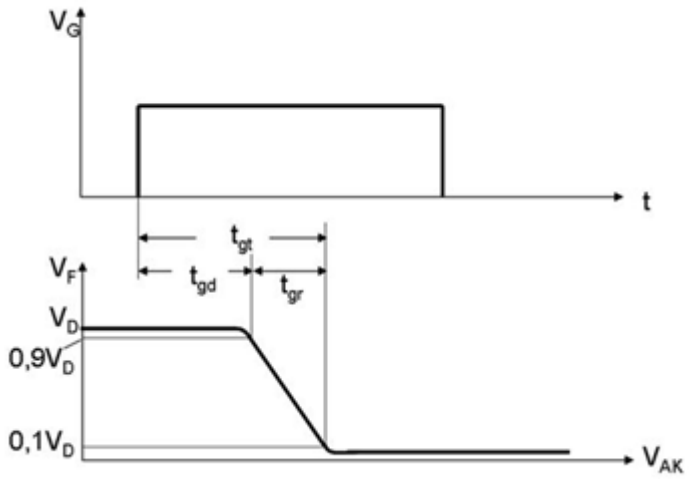
3.3.20 [Gate non-trigger voltage V_{GD} and Non-trigger current I_{GD}]

These trigger voltage and current values will not cause the thyristor to fire within the permissible operating temperature range. Inductive or capacitive interference in the triggering circuits must be kept below these values.

3.3.21 [Time definitions for triggering]

Fig. 3-7 shows the characteristics of gate trigger signal V_G and anode-cathode voltage V_{AK} which define the time intervals for the triggering process.

Figure 12: Time definitions for thyristor triggering



3.3.22 [Gate-controlled delay time t_{gd}]

Time interval between the start of a triggering pulse and the point at which the anode-cathode voltage falls to 90 % of its starting value. The datasheet specifies a typical value which is applicable, provided the following conditions are fulfilled:

- Square-wave gate pulse, duration 100 µs
- Anode-cathode starting voltage 0.5 V_{DRM}
- On-state current after firing approx. 0.1 I_{TAV} @ 85°C
- Junction temperature during firing approx. 25°C

3.3.23 [Gate controlled rise time t_{gr}]

Period within which the anode-cathode voltage falls from 90 % to 10 % of its starting value during firing.

3.3.24 [Gate current pulse duration t_{gt}]

The sum of the gate controlled delay time t_{gd} and the gate controlled rise time t_{gr}.

3.3.25 Thermal resistances $R_{th(x-y)}$ and thermal impedances $Z_{th(x-y)}$

For SEMIPACK® modules, thermal resistances/impedances are given for the heat flow between points "x" and "y". The indices used are as follows:

j - junction
c - case/base plate
s - heatsink
r - reference point
a - ambient

The contact thermal resistance case to heat sink $R_{th(c-s)}$ applies provided the assembly instructions are followed. In such cases, the given dependences of the internal thermal resistance junction to case $R_{th(j-c)}$ on the current waveform and the current flow angle should take into account any deviations from the

maximum instantaneous value of the mean junction temperature calculated. The values given in the datasheet tables apply to sinusoidal half waves only. Values for other current waveforms can be taken from the figures of the datasheet.

The thermal resistance junction to ambient $R_{th(j-a)}$ to be used in Fig. 1 and Fig.11 of the datasheet comprises the following components:

$$\mathbf{R_{th(j-a)} = R_{th(j-c)} + R_{th(c-s)} + N * R_{th(s-a)}}$$

where N: the number of thyristors or diodes operating simultaneously on one heat sink.

The thermal resistance $R_{th(s-a)}$ of the heat sink decreases as the following parameters increase: power dissipation, the cooling air flow rate, the number of SEMIPACK® modules mounted and the distance between the individual modules.

The transient thermal impedances in the SEMIPACK® modules $Z_{th(j-c)}$ and $Z_{th(j-s)}$ are shown in the diagrams Fig. 6 and Fig 14 of the datasheets as a function of the time t. For times > 1 s, the transient thermal impedance $Z_{th(s-a)}$ of the heat sink must be added to this in order to calculate the total thermal impedance. For this purpose, the datasheets for SEMIKRON heat sinks normally contain a diagram illustrating the given thermal impedance $Z_{th(s-a)}$ or $Z_{th(c-a)}$ as a function of the time t. When several components are being mounted on one heat sink, in order to calculate the transient thermal impedance of one component, the thermal heat sink impedance must be multiplied by the total number of components N.

3.3.26 Temperatures

The most important referential value for calculating limiting values is the maximum permissible junction temperature T_j. At most in the event of a circuit fault (e.g. when a fuse is activated) may this value be exceeded briefly (cf. "Surge on-state current"). Another important reference point for the permissible current capability is the case temperature T_c. In SEMIPACK® modules, the measuring point for T_c (Reference point/Reference temperature T_{cref}) is the hottest point of the baseplate beneath the hottest chip, measured through a hole in the heat sink. The heat sink temperature T_s is of particular interest for defining power dissipation and heat sink. In SEMIPACK® modules the measuring point for T_s (Reference point/Reference temperature T_{sref}) is the hottest point of the heat sink besides the baseplate, measured from above on the sidewall of the module (cf. IEC 60747-1 and IEC 60747-15). The permissible ambient conditions without current or voltage stress are described, among other things, by the maximum permissible storage temperature T_{stg}. The parameter T_{stg} is also the maximum permissible case temperature, which must not be exceeded as a result of internal or external temperature rise.

3.3.27 Mechanical limiting values

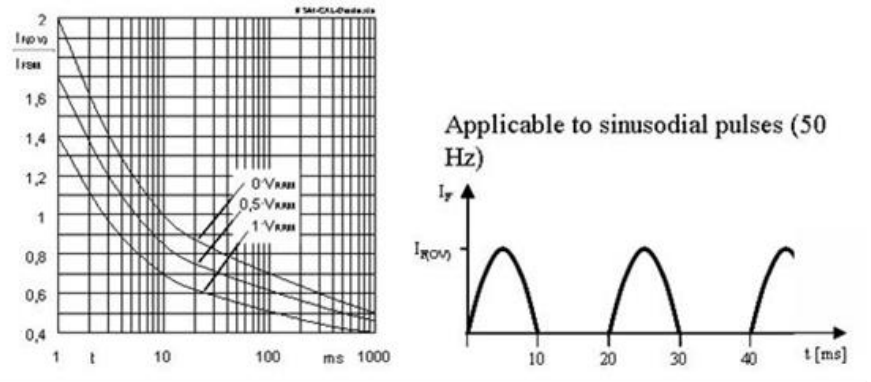
The limiting values for mechanical load are specified in the datasheets, e.g.:
M_s : Max. tightening torque to heat sink
M_t : Max. tightening torque to terminals
a : Max. permissible amplitude of vibration or shock acceleration in x, y and z direction.

If SEMIPACK® modules with no hard mould are to be used in rotating applications, the soft mould mass may come away and leak. In such cases, Please contact SEMIKRON for these applications.

4. Qualification

4.1 Surge overload current

Figure 13: Surge overload current vs. time



Peak value of overload current $I_{T(OV)}$ permissible under fault conditions normalised to the surge on-state current I_{TSM} shown as a function of the duration of the fault t. The parameter is the peak reverse voltage to be reapplied immediately after the fault current has ceased. For faults lasting longer than 10 ms the graph assumes the current waveform to be a series of half sinewaves of 8.3 or 10 ms duration occurring at a rate of one every 16.6 or 20 ms.

0· V_{RRM}: no reverse voltage reapplied,
½· V_{RRM}: a voltage equal to half the repetitive peak reverse voltage rating reapplied,
1· V_{RRM}: a voltage equal to the full repetitive peak reverse voltage rating reapplied.

4.2 Insulation test

The insulation voltage of SEMIPACK modules is a guaranteed value for the insulation between the terminals and the base plate. The limiting value 4.8 kV_{rms} specified for 1 s is subject to 100% production testing.
All terminals – including the gate connections - must be interconnected during dielectric testing. All specifications for the final products dielectric test voltage are described in the IEC publications IEC 60146-1-1.

4.3 Tests using change of temperature

Since the external contacts have a significantly higher thermal expansion coefficient than the silicon chip, it is apparent that temperature cycling, which stresses these external contacts, is in turn a particularly good test for checking the load cycling stability of the internal contacts. The test can be carried out by using the same methods as described in the above section for the testing for leaks in the encapsulation using thermal cycling. After the testing, the first criteria used for checking whether the contacts have withstood the stresses imposed, is to check the thermal resistance, but additionally the forward and reverse characteristics are checked.

4.4 Thermal cycling load tests using pulsed loading and constant cooling

Tests which use external heating and cooling of the component deviate from actual operation conditions in so far as here the component under test is uniformly heated and cooled, whereas in reality a varying temperature gradient occurs between the silicon chip and the outside. Therefore it is recommended, particularly for the type tests of a newly development component, that a further test method is used, which makes it possible in a short time to go through a large number of cycles giving similar stresses to those which occur in the actual working environment. To achieve this the component under test is brought in close contact with a water cooled heat sink, so that the case temperature is kept almost constant, and by applying short, high current pulses the silicon chip is cyclically heated up to almost its maximum allowable junction temperature. During the intervals between the pulses the junction cools down very rapidly. This method produces periodically a high temperature gradient between the silicon chip and the mounting surface.

4.5 Standard tests for qualification

The objectives of the test programme are:

1. To ensure general product quality and reliability.
2. To evaluate design limits by performing stress tests under a variety of test conditions.
3. To ensure the consistency and predictability of the production processes.
4. To assess process and design changes with regard to their impact on reliability.

Following table lists the standard tests for qualifications:

Figure 14: SEMIKRON standard test for product qualification

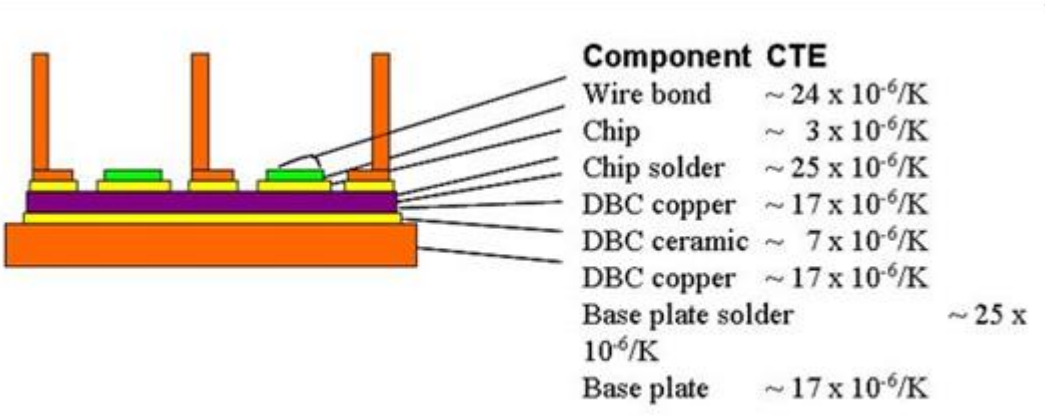
	Standard Test Conditions for	
Reliability Test	**MOS / IGBT Products:**	**Diode / Thyristor Products:**
High Temperature Reverse Bias (HTRB) *IEC 60747*	1000 h, 95% V_{DSmax}/V_{CEmax}, 125°C ≤ T_c ≤ 145°C	1000 h, DC, 66% of voltage class, 105°C ≤ T_c ≤ 120°C
High Temperature Gate Bias (HTGB) *IEC 60747*	1000 h, ± V_{GSmax}/V_{GEmax}, T_{vjmax}	not applicable
High Humidity High Temperature Reverse Bias (THB) *IEC 60068-2-67*	1000 h, 85°C, 85% RH, V_{DS}/V_{CE} = 80% V_{DSmax}/V_{CEmax}, max. 80V, V_{GE} = 0V	1000 h, 85°C, 85% RH, V_D/V_R = 80% V_{Dmax}/V_{Rmax}, max. 80V
High Temperature Storage (HTS) *IEC 60068-2-2*	1000 h, T_{stgmax}	1000 h, T_{stgmax}
Low Temperature Storage (LTS) *IEC 60068-2-1*	1000 h, T_{stgmin}	1000 h, T_{stgmin}
Thermal Cycling (TC) *IEC 60068-2-14 Test Na*	100 cycles, T_{stgmax} - T_{stgmin}	25 cycles, 100 cycles (capsule) T_{stgmax} - T_{stgmin}
Power Cycling (PC) *IEC 60749-34*	20.000 load cycles, ΔT_j = 100K	10.000 load cycles, 20.000 load cycles (capsule) ΔT_j = 100K
Vibration *IEC 60068-2-6 Test Fc*	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)	Sinusoidal sweep, 5g, 2 h per axis (x, y, z)
Mechanical Shock *IEC 60068-2-27 Test Ea*	Half sine puls, 30g, 3 times each direction (±x, ±y, ±z)	Half sine puls, 30g, 3 times each direction (±x, ±y, ±z)

More detail to the above specified quality test or specific test results are available upon request. A complete document is available for customer presentation. Please contact SEMIKRON SEMIPACK® Product Management.

4.6 Lifetime calculations

The lifetime of a power module is limited by mechanical fatigue of the package. This fatigue is caused by thermally induced mechanical stress caused by different coefficients of thermal expansion (CTE). This means that in the course of heating (power on) and cooling (power off) = temperature swing (power cycle), the materials expand differently due to their different CTEs. Since the materials are joined, they are unable to expand freely, leading to the aforementioned thermally induced mechanical stress.

Figure 15: Cross sectional view of SEMIPACK package, including the coefficients of thermal expansion (at 20 °C)



When temperature changes, the mechanical stresses that occur inside the different material layers lead to material fatigue. The bigger the temperature difference (ΔT), the more stress is induced. With every temperature cycle aging takes place. Wire bonding and solder layers are particularly affected by this. This aging results in small cracks which start at the edges and increase in the direction of the centre of the material with every power cycle that occurs. The higher the medium temperature T_{jm}, the faster the cracks grow, because the activating energy is higher.

The typical resulting failure picture from field returns is "lift off" of the wire bonds. This means that the cracks meet in the centre and open the connection in such a way that the wire bond is loose.

This shows that the lifetime is determined by the number of temperature cycles, which can be withstood by the module. In the 90's intensive investigations were carried in this area, including a research project known as the "LESIT study". One of the main findings of this study was the equation given below (4-1), which shows relationship between the number of cycles N_f and the junction temperature difference ΔT_j and the medium temperature T_{jm}.
SEMIPACK modules are based on the same design principles as the modules which were investigated in the course of the LESIT study. For this reason the LESIT results may be used for life time estimations. That said, the reliability of power modules has improved since the LESIT study was concluded, which is why the results of equation (4-1) can be seen as a worst-case scenario.

$$N_f = A \times \Delta T_j^{\alpha} \times \exp\left(\frac{E_a}{k_B \times T_{jm}}\right) \qquad (4\text{-}1)$$

With adjusted parameters for the Figure 17: "LESIT" curves for soldered contact modules, based on experimental results
$A = 3.025 \times 10^5$
$\alpha = -5.039$
$E_a = 9.891 \times 10^{-20}$ [J]
k_B = Boltzmann constant; ΔT_j and T_{jm} in [K]

Figure 17: "LESIT" curves for soldered contact modules, based on experimental results, shows the experimental results of the LESIT study (as bullet points) as well as the results of equation (4-1) as drawn lines.

Figure 16: Example of Tjm and ΔTj

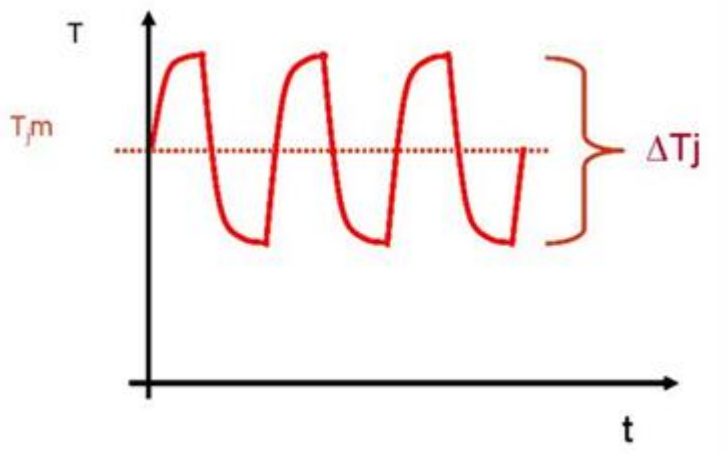


Figure 17: "LESIT" curves for soldered contact modules, based on experimental results

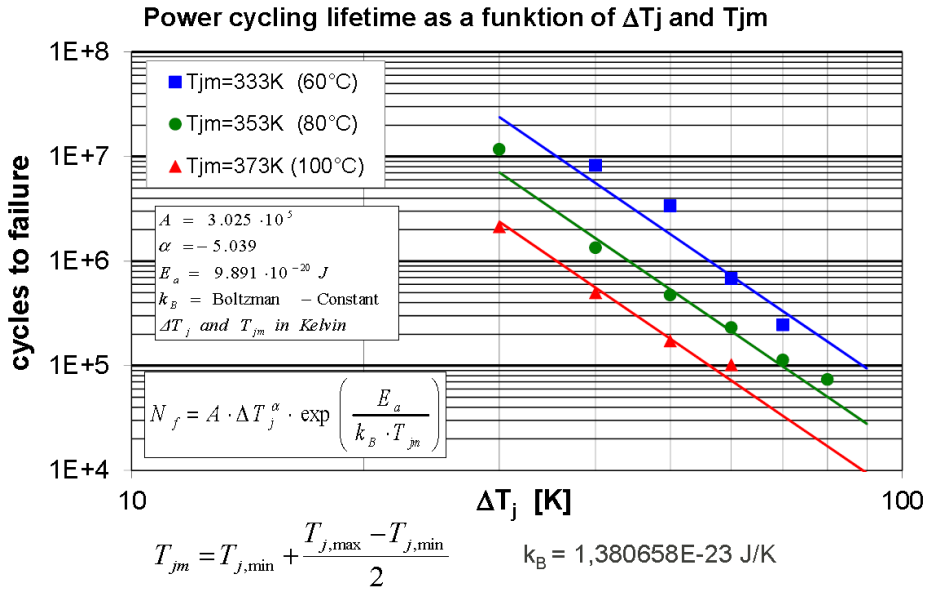
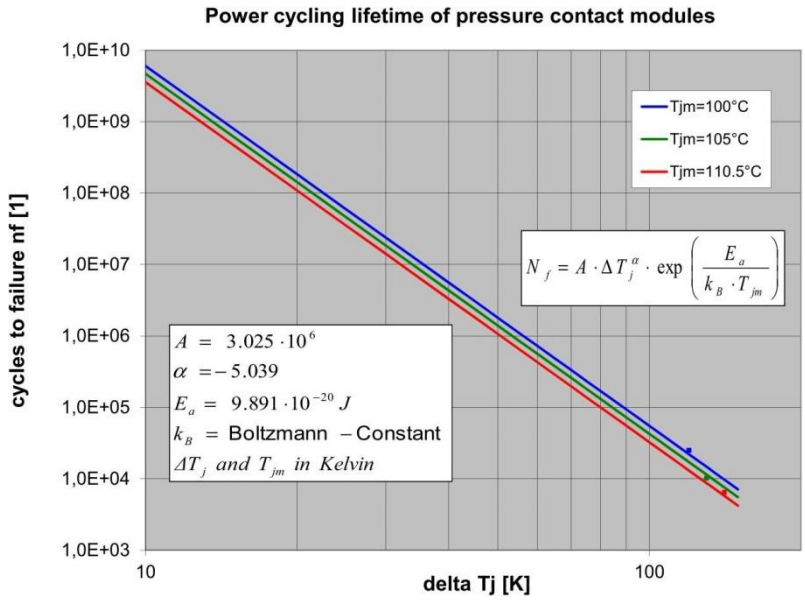


Figure 18: "LESIT" curves for pressure contact modules, based on experimental results*



* The data base for this lifetime curve is limited.

For further information on the lifetime calculations for power modules please refer to:
M. Held et.al., "*Fast Power Cycling Tests for IGBT Modules in Traction Application*"; Proceedings PEDS, pp 425 – 430, 1997 [1]

5. Application

The terms in [ ] apply solely to thyristors.

5.1 Voltage Class Selection

The table below contains the recommended voltage class allocations for the repetitive peak reverse voltages V_{RRM} [V_{DRM}] of SEMIPACK ® modules and rated AC input voltage V_{VN}.

Figure 19: Recommended voltage class allocations for the repetitive peak reverse voltages VRRM[VDRM]

Rated AC voltage L-L	Recommended peakreverse voltage
VDRM	V_{RRM}, [V_{DRM}] / V
60	200
125	400
250	800
380	1200
400	1400
440	1400
460	1600
500	1600
575	1800
660	2200
690	2200

As detailed in the technical explanations, the maximum permissible value for direct reverse voltages (continuous duty) across diode (V_R) [or thyristors (V_D, V_R)] in stationary operations is 0.7 V_{RRM} [0.7 V_{DRM}].

5.2 Overvoltage Protection

It is well known that single crystal semiconductor devices are sensitive to over-voltages. Every time their specified reverse voltage is exceeded it can lead to their destruction. It is therefore necessary to protect silicon diodes and thyristors against voltage transients however caused, i.e. the transient voltages must be reduced to values below the maximum specified limits for the semiconductor device.
A variety of well tried and tested components are suitable for the above suppression. The most important are:

- resistors and capacitors (RC snubber networks)
- varistors
- silicon avalanche diodes

The RC network operates by forming a series resonant circuit with existing inductances which transforms any steeply rising transient voltage into a damped sinewave of lower amplitude. The power of the voltage transient is converted from a high value of short duration to a lower value extending over a longer period of time.

All the other components listed above use non-linear characteristics. Their internal resistances reduce as the applied voltage increases. Together with the other resistances and inductances in the circuit, they build non-linear voltage dividers which allow low voltages to go through unattenuated, but clip high voltages above a defined level. The energy of the transient voltage is again spread over a longer period, and is almost completely absorbed by the suppression component.

The suppression components can be positioned on the a.c. side of the diode or thyristor stack, on the d.c. side, or across each semiconductor device in the circuit. The advantages and disadvantages of these various arrangements will be considered separately for each type of suppression component.
RC snubber circuits are often connected in parallel to the diode [thyristor] to provide protection from transient overvoltage, although in some cases varistors are used. Due to the RC circuit the rate of rise of voltage is limited during commutation, which reduces the peak voltages across the circuit inductors.
For higher circuit requirements, the RC circuit design should first be tested experimentally. The table below contains sample resistance and capacitance values recommended by SEMIKRON for standard line applications.

Table 4: Sample recommended resistance and capacitance values

	V_{VN}≤250V	V_{VN}≤400V	V_{VN}≤500V	V_{VN}≤660V
SKKx15 … 27	0.22µF 68Ω / 6W	0.22µF 68Ω / 6W	0.1µF 100Ω / 10W	- -
SKKx42 … 107	0.22µF 33Ω / 10W	0.22µF 47Ω / 10W	0.1µF 68Ω / 10W	0.1µF 100Ω / 10W
SKKx122 … 260 (on P3 heatsink)	0.22µF 33Ω / 10W	0.22µF 47Ω / 10W	0.1µF 68Ω / 10W	0.1µF 100Ω / 10W
SKKx122 … 260 (higher currents)	0.47µF 33Ω / 25W	0.47µF 33Ω / 25W	0.22µF 47Ω / 25W	0.22µF 68Ω / 50W

5.3 Overcurrent and Short Circuit Protection

If short circuit protection is required for the diodes, [thyristors], (ultra fast) semiconductor fuses are used. These are to be dimensioned on the basis of the forward current and i^2t value.

Other types of protection for high current circuits are, for example, fuses which isolate damaged diodes [thyristors] from the parallel connections. To protect components from statically non-permissible high overcurrents, it is possible to use magnetic or thermal overcurrent circuit breakers or temperature sensors on the heat sinks. Although these do not detect dynamic overload within a circuit. For this reason, temperature sensors are used mainly with forced air cooling in order to protect the diodes [thyristors] in the event of a fan failure.

5.4 Permissible Overcurrents

The permissible forward currents for short-time or intermediate operation, as well as for frequencies below 40 Hz are to be calculated on the basis of the transient thermal impedance or the thermal impedance under pulse conditions so that the junction temperature T_j does not exceed the maximum permissible value at any time.

5.5 FAQ for Applications

5.5.1 Difference between SKKT.../ and SKKT...B

Q: What is the difference between SEMIPACK thyristor modules with and without the extension B (for example SKKT57 and SKKT57B)?

A: The difference is the arrangement of the control connectors Gate (G) and Auxiliary Cathode (K), concerning SEMIPACK1 with 4 auxiliary connectors only.

For SKKT20 … SKKT107 : G1/K1 G2/K2
For SKKT20B … SKKT107B : G1/K1 K2/G2

5.5.2 Derating of rectifier current at higher frequencies

Q: Is a derating of the rectifier current necessary at higher frequencies?

A: Line rectifiers like diodes or thyristors are usable without current derating in a frequency range of 16.66Hz to 400Hz. Above this frequency is needed a derating, because of the normally neglected switching losses.

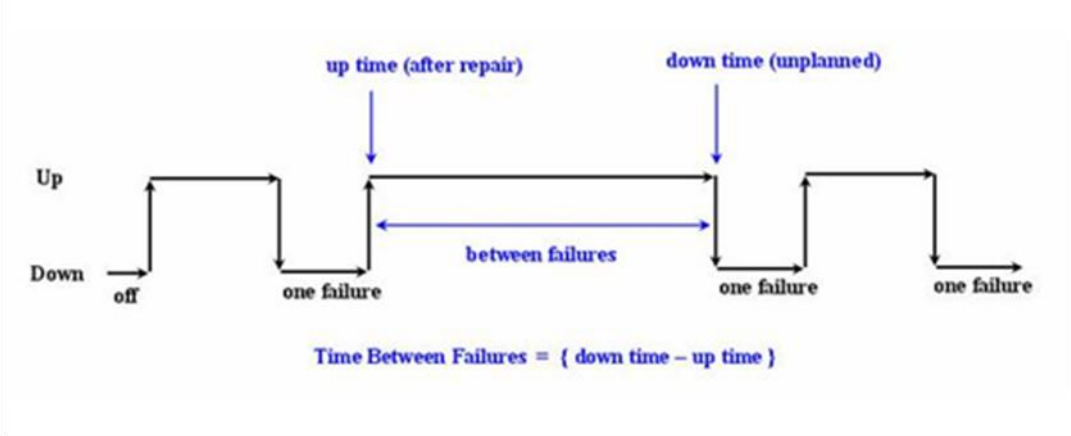
5.5.3 MTBF value

Failure rate is the frequency, with which an engineered system or component fails, expressed for example in failures per hour. It is often denoted as λ and is important in reliability theory.

$$\lambda = \text{FIT} = \frac{n_f}{N \cdot t}$$

n_f - Number of observed failures
N - Number of observed components
t - Observation time

Figure 20: Information about the calculation of reliability



In practice, the reciprocal rate MTBF is more commonly expressed and used for high quality components or systems.

Mean time between failures (MTBF) is the mean (average) time between failures of a system, and is often attributed to the "useful life" of the device i.e. not including 'infant mortality' or 'end of life' if the device is not repairable. Calculations of MTBF assume that a system is "renewed" i.e. fixed, after each failure, and then returned to service immediately after failure. The average time between failing and being returned to service is termed mean down time (MDT) or mean time to repair (MTTR).

More information: *http://en.wikipedia.org/wiki/Mean_Time_Between_Failures*

MTBF values given below are evaluated from the customer returns only, without any measurements. Therefore, the values are for reference only and cannot be guaranteed.

Figure 21: Estimated FIT and MTBF values of SEMIPACK products

Product	Fit	MTBF (x 10^8h)
Semipack 1	70	0,14
Semipack 2	50	0,2
Semipack 3	50	0,2
Semipack 4	50	0,2
Semipack 5	50	0,2

5.5.4 Why does SEMIKRON define the min. V_{GT} and I_{GT}, however some competitors give max. V_{GT} and I_{GT} values in their datasheets?

Due to the following reason SEMIKRON specifies I_{GT} and V_{GT} in datasheets as min. values:
In the chapter "Modules-Explanations-SEMIPACK" in our data sheet catalogue the definition of I_{GT} and V_{GT} is: Minimum values for square-wave triggering pulses lasting longer than 100µs or for d.c.. The values are necessary to fire a thyristor at T_{vj}=25°C properly. Therefore, we give the min. I_{GT} and V_{GT} values in our datasheets.
Max. I_{GT} and V_{GT} values given in competitor datasheets are sometimes called highest gate current/voltage, which cannot be exceeded in order to keep thyristor not firing. i.e. customer can apply max. I_{GT} and V_{GT} values to the thyristor without firing it.

Both definitions have the same meaning and are only expressed in a different way.

5.5.5 Resistance of semiconductor:

It is impossible to measure the resistance of a semiconductor with an Ohm meter.
Reasons are the leakage current and the nonlinear characteristics of semiconductor, which can vary over several decades
The gate - cathode terminals can be checked with a "diode" function of a multimeter, but not with the resistor function.

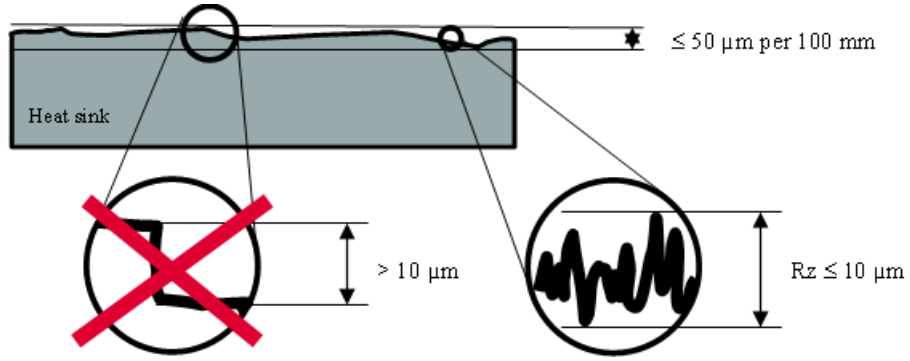
6. Mounting Instruction

6.1 Heatsink and Surface Specifications, Preparation

In order to ensure good thermal contact and to obtain the thermal contact resistance values specified in the datasheets, the contact surface of the heat sink must be clean and free from dust particles. It is useful to clean the mounting surface of the heat sink with wipes and an alcohol cleaner, e.g. isopropanol, right before the mounting process. The following mechanical specifications have to be met:

Unevenness of heat sink mounting area must be ≤ 50µm per 100 mm (DIN EN ISO 1101)
Roughness Rz: < 10 µm (DIN EN ISO 4287)
No steps > 10 µm (DIN EN ISO 4287)

Figure 22: Heat sink surface specification



6.2 Applying Thermal Paste

SEMIKRON recommends to use stencil printing in order to apply thermal interface material. For SEMIPACK we recommend thermal paste thickness in the range from 50 µm to 100 µm. Further information about applying thermal interface material you find in Thermal Paste Application (AN 18-001) [2].
Applying thermal paste by means of roller is not recommended for mass production as reproducibility of an optimized thermal paste thickness cannot be guaranteed.

6.3 Assembly Process

6.3.1 Mounting torque on heat sink M_S

To secure SEMIPACK modules, the use of steel screws (DIN 7984-8.8) in combination with suitable washers and spring lock washers or combination screws is strongly recommended. The specified torque value must be observed.

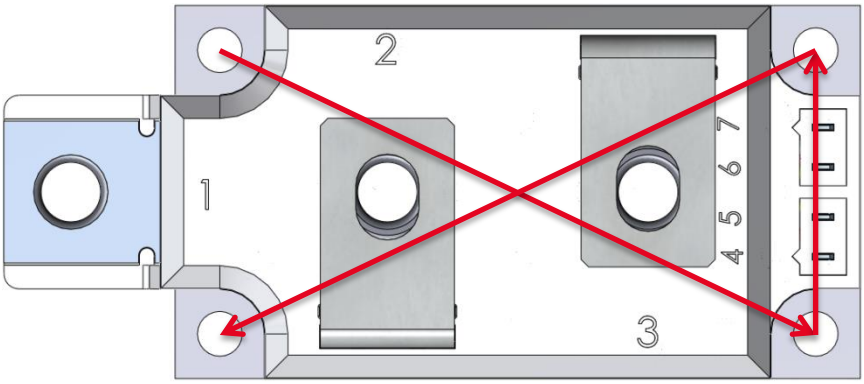
Table 5: Mounting details

	SEMIPACK 0 soldered modules	SEMIPACK 1, 2 soldered modules	SEMIPACK 3 soldered / bonded modules	SEMIPACK 3, 4, 5 pressure contact modules	SEMIPACK 6 pressure contact modules
Mounting screw	2 pcs M4	2 pcs M5 x 18 (DIN 7984-8.8)	4 pcs M5 x 18 (DIN 7984-8.8)	4 pcs M5 x 20 (DIN 7984-8.8)	4 pcs M6 x 20 (DIN 7984-8.8)
Mounting speed	-	max. 300 rpm	max. 300 rpm	max. 300 rpm	max. 300 rpm
Pre-tightening torque	-	0.6 Nm	0.6 Nm	0.6 Nm	0.6 Nm
Final torque M_S	1.275–1.725 Nm	4.25–5.75 Nm	4.25–5.75 Nm	4.25–5.75 Nm	5.1–6.9 Nm

A pre-tightening torque and retightening to the given torque value is recommended. For the screwing process the speed has to be limited and soft torque limitation is recommended to avoid torque peaks, which may occur with pneumatic screwdrivers. Calibrated screwdrivers (manual screwdriver or electrical screwdriver) are recommended.

The screws must be tightened in diagonal order with equal torque in several steps until the specified torque value MS has been reached. An example of the diagonal mounting order is shown in Figure 23.

Figure 23: Example of mounting order



6.4 Mounting hardware for SEMIPACK® modules

6.4.1 Available mounting hardware

There are complete kits available for SEMIPACK® 1, 2, 3 (bonded or pressure contact) and 4. No kits are available for SEMIPACK 0, 5 and 6.

Table 6: Mounting hardware for SEMIPACK modules

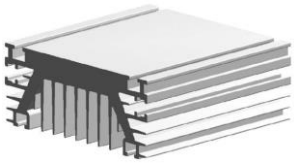
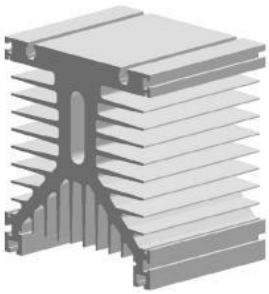
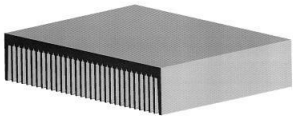
Hardware needed for one SEMIPACK®	SEMIPACK® 1 a:SKKD/E b:SKKT/H/L	SEMIPACK® 2	SEMIPACK® 3 bonded and pressure contact modules	SEMIPACK® 4
Gate female plug:	b: 2 pcs. 2.8 x 0.8	4 pcs. 2.8 x 0.8	a: 4 pcs. 2.8 x 0.8	2 pcs. 2.8 x 0.8
Insulating sleeve:	b: 4 pcs.	-	-	-
Double plug caps:	-	2 pcs. (right + left)	a: 2 pcs. (right + left)	1 pc. (right)
Baseplate screws:	2 pcs. M5 x 18 socket head	2 pcs. M5 x 18 socket head	a: bonded modules: 4 pcs. M5 x 18 socket head, b: pressure contact modules: 4 pcs. M5 x 20 socket head	4 pcs. M5 x 18 socket head, modules on heat sink P3: 4 pcs. M5 x 20 socket head
Terminal screws:	3 pcs. M5 x 10 pozidrive head	3 pcs. M6 x 12 pozidrive head	a: 3 pcs. M8 x 16 hexagon head	2 pcs. M10 x 50 with two nuts M10
Washers:	captive	(3 pcs. Ø6.4mm)	captive	(2 pcs. Ø10.5mm)
Spring washers:	captive	(3 pcs. Ø6.4mm)	captive	2 pcs. Ø10.5mm
Part No. of the complete kit:	For 12 modules: a: 33704200 b: 33403900	For 8 modules: 33404000	For 3 modules: a: 33404100	For 3 modules: 33404500

Two different double plug caps are available. The double plug cap with right nose is used for terminals 4 and 5 of SEMIPACK 2, 3, 4 and 5. The double plug cap with left nose is used for terminals 6 and 7 of SEMIPACK 2, 3, 5 and 6.

The kits contain baseplate and terminal screws, gate plugs, insulating sleeves and double plug caps, depending on the ordered type of the module.

6.4.2 Available heatsinks

Table 7: Heatsink types

	R4A	P3	P21
			
SEMIPACK® 1	X	X	X
SEMIPACK® 2		X	X
SEMIPACK® 3		X	X
SEMIPACK® 4		X	X
SEMIPACK® 5			X
SEMIPACK® 6			X

Integrated rails for easy mounting of the modules. Heatsinks are available in different lengths. For further details please see the heatsink datasheets on our website www.semikron.com.

7. Laser marking

Figure 24: Laser marking on modules

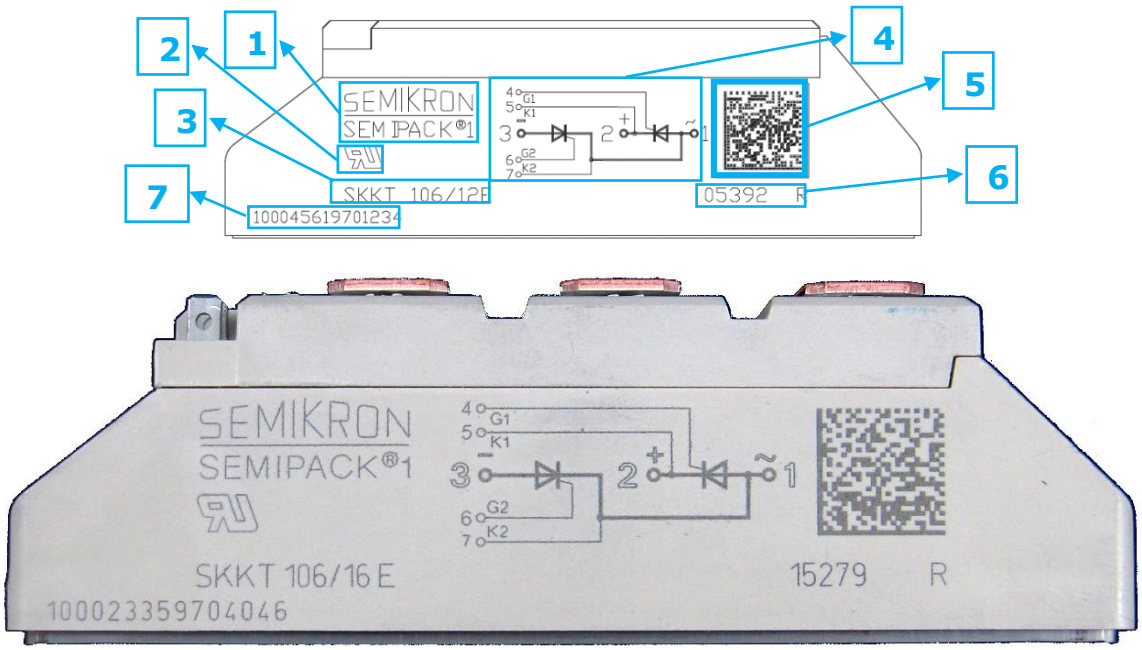


Table 8: Laser marking description of SEMIPACK 1 module	
1	SEMIKRON logo, with product line designation “SEMIPACK®”
2	UL logo, SEMIPACK is UL recognised, file name: E63532
3	Type designation
4	Circuit diagram
5	Data Matrix Code
6	Date code – 5 digits: YYWWL (L = Lot of same type per week)
7	Code for internal use. This code is not necessarily on each module.

8. Data matrix code

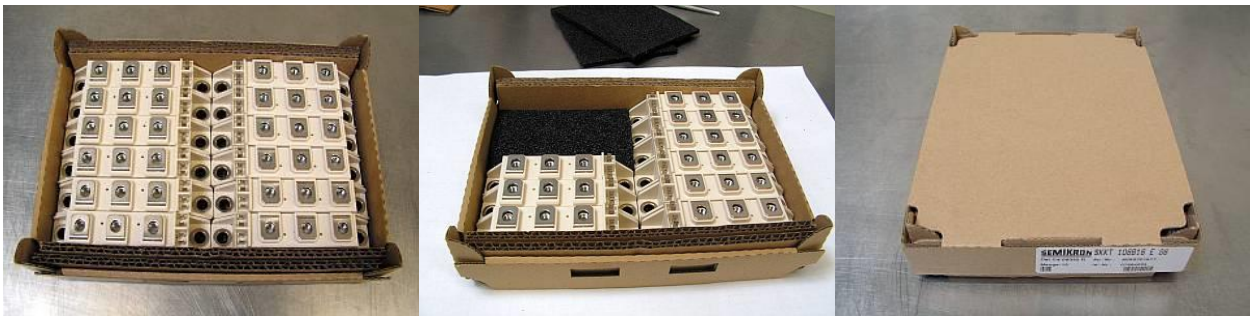
The Data Matrix Code contains the following information:

- Type description
- Part number
- Lot number
- Measurement number
- Measurement line number
- Production tracking number
- Datecode
- Sequential lot number (lot of same type per week)

9. Packaging specification

9.1 Packing boxes

Figure 25: Standard packing boxes for SEMIPACK 1 modules (12 pieces)



Full box *Partially filled box* *Closed box with label*

Figure 26: Standard packing boxes for SEMIPACK 2 modules (8 pieces)

Full box *Closed box with label*

Figure 27: Standard packing boxes for SEMIPACK 3 and 4 modules (3 pieces)

Full box *Closed box with label*

Figure 28: Standard packing boxes for SEMIPACK 5 modules (2 pieces)

Full box *Partially filled box* *Closed box with label*

Figure 29: Standard packing boxes for SEMIPACK 6 modules (1 piece)

Full box *Closed box with label*

9.2 Package label content

Figure 30: SEMIPACK packing boxes label

1 - SEMIKRON logo
2 - Type designation
3 - Date code
4 - SEMIKRON part number - also as a bar code
5 - Quantity - also as a bar code

10. Description of the figures in the datasheet

10.1 SEMIPACK® thyristor modules

Fig. 1
Left: Power dissipation P_{TAV} as a function of the mean on-state current I_{TAV} for smoothed d.c. (cont.), sinusoidal half waves (sin. 180) and square-wave pulses (rec. 15...180) for a single thyristor (typical values)
Right: Max. permissible power dissipation P_{TAV} as a function of the ambient temperature T_a (temperature of the cooling air flow) for the total thermal resistances (junction to ambient air) $R_{th(j-a)}$ (typical values)

Fig. 2
Left: Total power dissipation P_{TOT} of a SEMIPACK® module used in an a.c. controller application (W1C a.c. converter) as a function of the maximum rated rms current I_{RMS} at full conduction angle (typical values)
Right: Max. permissible power dissipation P_{TOT} and resultant case temperature T_c as a function of the ambient temperature T_a; Parameter: Heatsink thermal resistance case to ambient air $R_{th(c-a)}$ (including the total contact thermal resistance 1/2 $R_{th(c-s)}$ between a SEMIPACK® module and the heat sink. For the power dissipation given on the l.h.s. vertical, the case temperatures given on the r.h.s. vertical are permissible

Fig. 3
Left: Total power dissipation P_{TOT} of 2 SEMIPACK® modules in a two-pulse bridge connection (B2C) as a function of the output direct current I_D at full conduction angle for resistive (R) and inductive (L) load (typical values)
Right: Max. permissible power dissipation P_{TOT} and resultant case temperature T_c as a function of the ambient temperature T_a; Parameter: Heat sink thermal resistance case to ambient air $R_{th(c-a)}$ (including the total contact thermal resistance 1/4 $R_{th(c-s)}$ between a SEMIPACK® module and the heat sink. For the power dissipation given on the l.h.s. vertical, the case temperatures given on the r.h.s. vertical are permissible

Fig. 4
Left: Total power dissipation P_{TOT} of 3 SEMIPACK® modules in a six-pulse bridge connection (B6C) or in an a.c. controller connection (W3C) as a function of the direct output current I_D at full conduction angle resistive (R) and inductive (L) load (typical values)
Right: Max. permissible power dissipation P_{TOT} and resultant case temperature T_c as a function of the ambient temperature T_a; Parameter: Heat sink thermal resistance case to ambient air $R_{th(c-a)}$ (including the total contact thermal resistance 1/6 $R_{th(c-s)}$ of a SEMIPACK® module and the heat sink. For the power dissipation given on the l.h.s. vertical, the case temperatures given on the r.h.s. vertical are permissible

Fig. 5
Typical recovery charge Q_{rr} for the max. permissible junction temperature as a function of the rate of fall of the forward current $-di_T/dt$ during turn-off, Parameter: Peak on-state current I_{TM} before commutation

Fig. 6
Transient thermal impedances junction to case $Z_{th(j-c)}$ and junction to sink $Z_{th(j-s)}$ for smoothed d.c. as a function of the time t elapsed after a step change in power dissipation, for a single thyristor

Fig. 7
Forward characteristics: on-state voltage V_T as a function of the on-state current I_T; typical and maximum values for T_j = 25 °C and T_{jmax}

Fig. 8
Surge current characteristics: Ratio of permissible overload on-state current $I_{T(OV)}$ for 10 ms to surge on-state current I_{TSM}, shown as a function of the load period t; Parameter: Ratio V_R / V_{RRM} of the reverse voltage V_R, which lies between the given sinusoidal half waves, to the peak reverse voltage V_{RRM}

Fig. 9
Gate voltage V_G as a function of the gate current I_G, indicating the regions of possible (BMZ) and certain (BSZ) triggering for various junction temperatures T_j. The current and voltage values of the triggering pulses must lie within the range of certain (BSZ) triggering, but the peak pulse power P_G must not exceed that given for the pulse duration t_p. Curve 20 V; 20 Ω is the output characteristic of suitable trigger equipment.

10.2 SEMIPACK® diode modules

Fig. 11
Left: Mean power dissipation P_{FAV} as a function of the mean continuous forward current I_{FAV} for smoothed d.c. (cont.), sinusoidal half waves (sin. 180) and square-wave pulses (rec. 15...180) for a single diode (typical values)
Right: Max. permissible power dissipation P_{FAV} as a function of the ambient temperature T_a (temperature of the cooling air flow) for different total thermal resistances (junction to ambient air) $R_{th(j-a)}$ (typical values)
Fig. 12
Left: Total power dissipation P_{TOT} of 2 SEMIPACK® modules in a two-pulse bridge connection (B2C) as a function of the output direct current I_D (typical values)
Right: Max. permissible power dissipation P_{TOT} and resultant case temperature T_c as a function of the ambient temperature T_a; Parameter: Heat sink thermal resistance case to ambient air $R_{th(c-a)}$ (including the total contact thermal resistance 1/4 $R_{th(c-s)}$ between a SEMIPACK® module and the heat sink. For the power dissipation given on the l.h.s. vertical, the case temperatures given on the r.h.s. vertical are permissible
Fig. 13
Left: Total power dissipation P_{TOT} of 3 SEMIPACK® modules in a six-pulse bridge connection (B6C) as a function of the direct output current I_D (typical values)
Right: Max. permissible power dissipation P_{TOT} and resultant case temperature T_c as a function of the ambient temperature T_a; Parameter: Heat sink thermal resistance case to ambient air $R_{th(c-a)}$ (including the total contact thermal resistance 1/6 $R_{th(c-s)}$ between a SEMIPACK® module and the heat sink. For the power dissipation given on the l.h.s. vertical, the case temperatures given on the r.h.s. vertical are permissible

Fig. 14
Transient thermal impedances junction to case $Z_{th(j-c)}$ and junction to heat sink $Z_{th(j-s)}$ of a single diode for smoothed d.c. as a function of the time t elapsed after a step change in power dissipation

Fig. 15
Forward characteristics: forward voltage V_F as a function of the forward current I_F; typical and maximum values for T_j = 25 °C and T_{jmax}

Fig. 16
Surge current characteristics: Ratio of permissible overload on-state current $I_{T(OV)}$ to surge on-state current I_{TSM} for 10 ms as a function of the load period t; Parameter: Ratio V_R / V_{RRM} of the reverse voltage V_R, which lies between the given sinusoidal half waves, to the peak reverse voltage V_{RRM}

Additional figures for special types may be available on request.
Please direct all requests and questions to SEMIKRON SEMIPACK® Product Management.

11. List of Figures

12. Symbols and Terms

Letter Symbol	Term
$(di/dt)_{cr}$	Critical rate of rise of on-state current
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage
a.c., AC	Alternating current
Al_2O_3	Aluminium oxide
AlN	Aluminium nitride
BMZ	The region of possible triggering
BSZ	The region of certain triggering
CTE	Coefficient of thermal expansion
d.c., DC	Direct current
DCB, DBC	Direct Copper Bonding, also Direct Bonding Copper, a type of substrate
di/dt	Change of current per time
DIN	Deutsches Institut für Normung e.V. (DIN; in English, the German Institute for Standardization)
dv/dt	Change of voltage per time
EN	European Standard
FIT	The Failures In Time (FIT) rate of a device is the number of failures that can be expected in one billion (10^9) device-hours of operation
i^2t	i2t value
I_{DD}	Forward off-state current (thyristor)
IEC	International Electrotechnical Commission (standard)
$I_{F(OV)}$	Overload forward current
I_{FAV}	Mean forward current
I_{FRMS}	RMS forward current
I_{FSM}	Surge forward current
I_{GD}	Gate non-trigger current
I_{GT}	Minimum guaranteed gate trigger current
I_H	Hold current
I_L	Latching current
I_{RD}	Direct reverse current
I_{RMS}	Maximum r.m.s current of a complete AC-controller circuit
ISO	International Organization for Standardization

$I_{T(OV)}$	Overload on-state current
I_{TAV}	Mean on-state current
I_{TRMS}	RMS on-state current
I_{TSM}	Surge on-state current
k_B	Boltzmann constant
l.h.s.	Left-hand side
MDT	Mean down time
MTBF	Mean time between failures
MTTR	Mean time to repair
N	Maximum number of serie-connected silicon elements
P_F	Forward power dissipation
P_{FAV}	Mean forward power dissipation
P_T	On-state power dissipation
P_{TAV}	Mean on-state power dissipation
P_{tot}	Total power dissipation
Q_{rr}	Reverse recovery charge
r.h.s.	Right-hand side
r_T	On-state slope resistance, forward slope resistance
$R_{th(c-a)}$	Thermal resistance case to ambient
$R_{th(c-s)}$	Thermal resistance case to heat sink
$R_{th(j-a)}$	Thermal resistance junction to ambient
$R_{th(j-c)}$	Thermal resistance junction to case
$R_{th(j-r)}$	Thermal resistance junction to reference point (temperature sensor)
$R_{th(j-s)}$	Thermal resistance junction to heat sink
$R_{th(s-a)}$	Thermal resistance heat sink to ambient
R_z	Roughness
T	Temperature
t	Time
T_a	Ambient temperature
T_c	Case temperature
t_f	Fall time
t_{gd}	Gate controlled delay time
t_{gr}	Gate controlled rise time
t_{gt}	Gate current pulse duration

t_{hw}	Duration of a half sinewave
T_j	Junction temperature
T_{jm}	The medium temperature
t_q	Circuit commutated turn-off time (thyristor)
T_s	Heatsink temperature
T_{stgmax}	Maximum storage temperature
T_{stgmin}	Minimum storage temperature
UL	Underwriters Laboratories, a safety consulting and certification company
UPS	Uninterruptible power supply
$V_{(TO)}$	Treshold voltage Thyristor
V_{DRM}	Repetitive peak off-state voltage
V_F	Forward voltage
V_G	Gate voltage
V_{GE}	Gate-emitter voltage
V_{isol}	Insulation test voltage
V_R	(Direct) reverse voltage
V_{RRM}	Repetitive peak reverse voltage
V_T	On-state voltage (thyristor)
$V_{T(TO)}$	Treshold voltage Thyristor
$Z_{th()}$	Transient thermal impedance
ΔT	Temperature difference
Θ	Conduction angle
λ	Failure rate

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [3].

13. References

[1] M. Held et.al., "*Fast Power Cycling Tests for IGBT Modules in Traction Application*"; Proceedings PEDS, pp 425 – 430, 1997
[2] https://www.semikron.com/dl/service-support/downloads/download/00581004-0/
[3] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", ISLE Verlag 2015, ISBN 978-3-938843-83-3

14. History

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